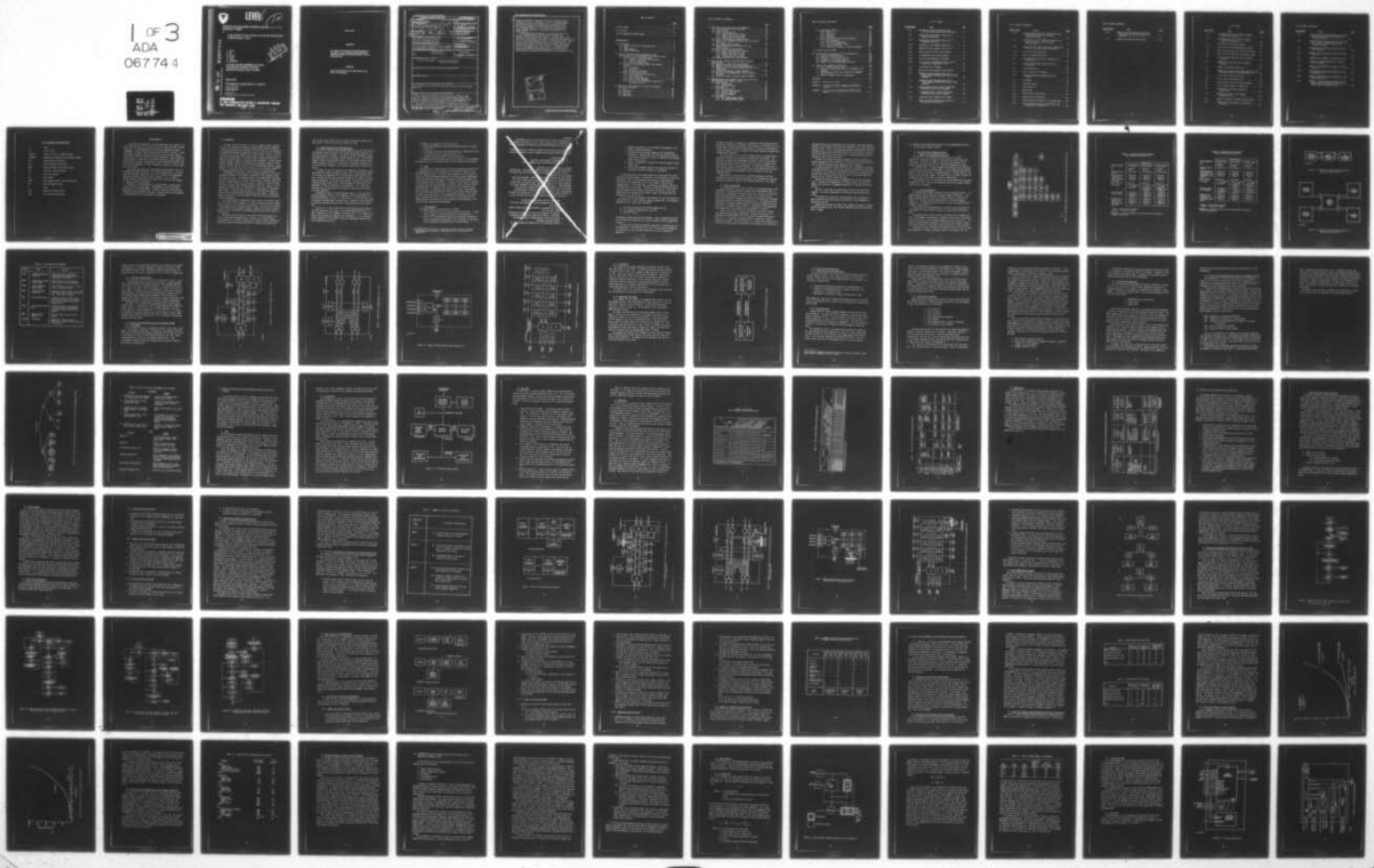
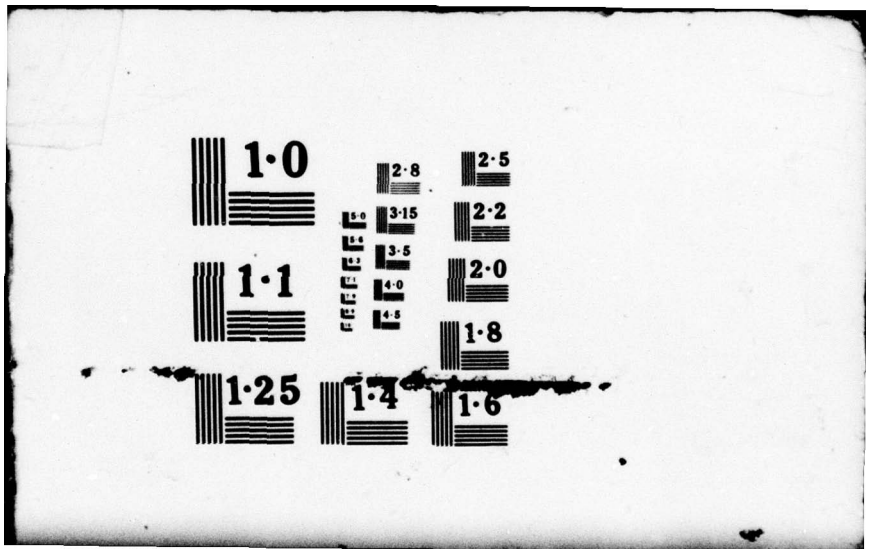
AD-A067 744 BATTELLE COLUMBUS LABS OHIO F/G 9/2
A PRELIMINARY STUDY OF BUILT-IN-TEST FOR THE MILITARY COMPUTER --ETC(U)
MAR 79 J B CLARY, A JAI, S WEIKEL, R SOEKS DAAG29-76-D-0100
UNCLASSIFIED CORADCOM-76-0100-F NL

1 OF 3
ADA
067744




1·0
1·1
1·25
1·4
1·6
1·8
2·0
2·2
2·5
2·8
3·15
3·5
4·0
4·5

LEVEL II

12

RESEARCH AND DEVELOPMENT TECHNICAL REPORT
CORADCOM-76-0100-F

A PRELIMINARY STUDY OF BUILT-IN-TEST FOR THE MILITARY COMPUTER FAMILY (MCF)

J. Clary
A. Jai
S. Weikel
R. Saeks
D. Siewiorek

SYSTEMS AND MEASUREMENTS DIVISION
THE RESEARCH TRIANGLE INSTITUTE
RESEARCH TRIANGLE PARK, NC 27709

March 1979

Final Report for Period 14 Feb. 78 - 16 Oct 78

PREPARED FOR
CENTER FOR TACTICAL COMPUTER SYSTEMS

CORADCOM
US ARMY COMMUNICATION RESEARCH & DEVELOPMENT COMMAND
FORT MONMOUTH, NEW JERSEY 07703

NOTICES

Disclaimers

The citation of trade names and names of manufacturers in this report is not to be construed as official Government indorsement or approval of commercial products or services referenced herein.

Disposition

Destroy this report when it is no longer needed. Do not return it to the originator.

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: CORADCOM-76-0100-F	2. GOVT ACCESSION NO. / 3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle): A Preliminary Study of Built-In-Test for the Military Computer Family (MCF),	5. TYPE OF REPORT & PERIOD COVERED: Final Report, 14 Feb 78 - 16 Oct 78,
	6. PERFORMING ORG. REPORT NUMBER: RTI/1600/00-05F
7. AUTHOR(s): J. Clary, A. Mahajan, S. Weikel, R. Saeks, and D. Siewiorek	8. CONTRACT OR GRANT NUMBER(s): DAAG29-76-D-0100, D.O. # 0781
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Systems and Measurements Division, The Research Triangle Institute, Research Triangle Park, NC 27709	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 612779.H62.01.11.00R410Z-8
11. CONTROLLING OFFICE NAME AND ADDRESS: Test Measurement & Diagnostic Systems Div, CENTACS, US Army Communications Research & Dev. Command, Fort Monmouth, NJ 07703	12. REPORT DATE: March 1979 / 13. NUMBER OF PAGES: 243p.
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Same	15. SECURITY CLASS. (of this report): UNCLASSIFIED / 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Distribution Statement: Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Fault Detection, Fault Isolation, Fault Repair, Built-In-Test, Performance Monitoring

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This study has addressed the use of built-in-test (BIT) for fault detection, isolation, and repair in the Military Computer Family (MCF). Particular emphasis was given to the identification and assessment of BIT techniques applicable to the MCF-AN/UYK-41(V). The MCF-AN/UYK-41(V) is software compatible with Digital Equipment Corporation's PDP-11/70.

The approach taken in this study was to assume a fault population, predict where in the system these faults are most likely to occur and → next page

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

407 080

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

79 04 20 013

LB

develop a rationale for deploying built-in fault detection and localization resources accordingly. The fault population assumed included both stuck-at and transient faults. It was determined using a failure prediction program based on MIL-HDBK-217B that for related computers, it is likely that 60% of all faults will occur in memory, 30% will be in the CPU and the remainder will happen throughout the rest of the computer including the power supply.

A unified built-in-test approach with appropriate inter-level and user communications was identified which provides fault detection coverage at the module, chassis, and system levels. The required BIT resources were characterized at each hierarchical level with the intent of serving as the basis for modifying the MCF-AN/UYK-41(V) form, fit, and function specifications to include built-in-test. Using state-of-the-art digital hardware including microprocessors, it was predicted that with 10 to 30% additional BIT hardware, approximately 80-95% of all assumed faults can be detected. To satisfy the MCF objective of minimizing false module pulls and in keeping with the proposed MCF two-level maintenance philosophy on-site, off-line module/chassis testing should be considered as a testing adjunct to BIT.

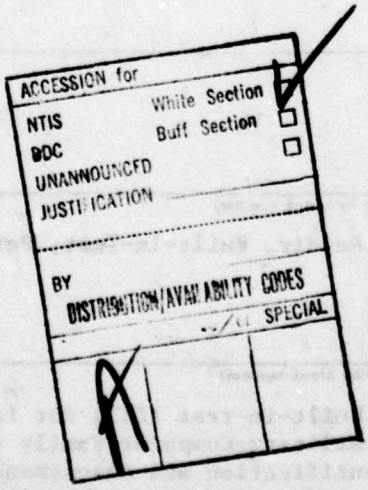


TABLE OF CONTENTS

TABLE OF CONTENTS (CONTINUED)

TABLE OF CONTENTS (CONTINUED)

LIST OF FIGURES

LIST OF FIGURES (CONTINUED)

LIST OF FIGURES (CONTINUED)

LIST OF TABLES

LIST OF TABLES (CONTINUED)

LIST OF ACRONYMS AND ABBREVIATIONS

A	Space
BIT	Built-In-Test
CENTACS	Center for Tactical Computer Systems
CORADCOM	Communication Research and Development Command
CMU	Carnegie-Mellon University
DEC	Digital Equipment Corporation
ECBIT	Expansion Chassis Level Built-In-Test
ESS	Electronic Switching System
F^3	Form, Fit, Function
FR	Failure Rate
MCBIT	Main Computer Chassis Level Built-In-Test
MCF	Military Computer Family
P	Power
SBIT	System Level Built-In-Test
STAR	Self Testing and Repairing

ACKNOWLEDGMENTS

This report was prepared for the Test Measurement and Diagnostic Systems (TMDS) Division of the Center for Tactical Computer Systems (CENTACS) under the U. S. Army Communications Research and Development Command (CORADCOM). Technical direction was provided by Messrs. Richard A. Sacane and George E. Burbank of TMDS and the joint services Military Computer Family (MCF) Built-In-Test (BIT) Selection Committee. Special thanks are given to Messrs. Bruno Witte of the Naval Ocean System Center (NOSC) and Bill Keiner of the Naval Surface Weapons Center (NSWC) both members of the BIT Selection Committee, for their illuminating thoughts on digital computer built-in-test.

This report was prepared by the Systems and Measurements Division of the Research Triangle Institute. The Project Leader was Mr. J. B. Clary under the laboratory supervision of Dr. R. A. Whisnant with programmatic assistance provided by Division Senior Engineer, Mr. R. D. Alberts. Primary technical contributions were made by RTI technical staff members, Dr. Atul Jai and Mr. Scott Weikel.

In addition to RTI personnel, Dr. Dan Siewiorek of Carnegie-Mellon University and Dr. Richard Saeks of Texas Tech University contributed significantly to the study effort. Professor Siewiorek provided valuable technical guidance throughout the study. Professor Saeks was instrumental in identifying MCF analog subsystem BIT requirements.

1.0 INTRODUCTION

The Army, through the Center for Tactical Computer Systems (CENTACS), Office of the Communications Research and Development Command (CORADCOM), is working cooperatively with the Navy and the Air Force on a new approach to developing and acquiring computers for the military [1]-[4]. The effort is known as the Military Computer Family (MCF) Program. The Military Computer Family Program goal is to provide defense system developers with a software-compatible family of standard, modular computers. The MCF program stresses software compatibility between prior generation computers at the level a programmer needs to know to write time-independent machine language programs. At the same time, the MCF concept calls for hardware compatibility through standardized Form, Fit and Function (F^3) specifications.

A consequence of being able to use existing software and state-of-the-art modular hardware is the potential reduction in total computer system life cycle cost (LCC). An important aspect of the proposed MCF procurement procedure with potential LCC savings is the concept of hardware vendor warranties. The MCF hardware warranty concept is viewed as a means of reducing logistic support costs through improved reliability. Implicit in this approach is the necessity of 1) knowing with a high degree of confidence that a module is not performing properly, 2) identifying which module is faulty, and 3) effecting repair through module replacement. To meet this need, an effective and efficient means of detecting and locating hardware faults is necessary.

The present study has addressed the use of built-in-test (BIT), couched in a unified testing framework, as a means of monitoring system performance and aiding in fault detection and isolation. Built-in-test as defined in this study refers to computer hardware, firmware and software resources which exist for the purpose of performance monitoring and fault detection and isolation.

The nature of built-in-test is such that it must be considered very early in the system conceptual phase. Further, it is essential that a unified approach to testing be established in order to insure maximum fault detection coverage at minimum additional BIT hardware and software cost.

This, in turn, must be done within an overall maintenance framework which makes sense in view of the plans and objectives of MCF.

1.1 General Discussion of Study Objectives

The Military Computer Family program addresses the need within DOD for new generation digital hardware while maintaining software compatibility with prior generation machines. In addition, the MCF concept goes beyond the transportability of software from old machines to new. Under the MCF program, a whole new procurement process is made possible through modular hardware computer structures. In particular, the modular hardware structure of MCF allows components to be procured simultaneously from multiple sources.

In order to insure the success of this competitive procurement process and to motivate vendors to produce reliable form, fit and function compatible designs, MCF components will be procured with vendor-backed warranties. The MCF warranty concept provides incentives for vendors to produce reliable components. At the same time, however, it places the burden of identifying faulty modules with a very high degree of confidence on the government in order for warranties to be exercised. It is, therefore, essential that available means be provided for identifying and locating faulty MCF components.

An additional aspect of the MCF warranty concept is the necessity of measuring component on-time if the components are to be warrantied for a pre-determined number of hours. A later section of this report deals with the elapsed time measurement question which, in addition to being important for warranty validation, may be useful in fault prediction and localization.

Finally, it is vital for MCF users to know system operating capabilities and limitations at all times. On-line performance monitoring is of utmost importance to field commanders and others who rely on computer systems to provide them with combat-critical information. It is, therefore, a primary objective of BIT for MCF to meet this requirement through timely fault detection and alerting.

In summary, the objectives of BIT for MCF are:

1. To provide continuous system monitoring and indication of system malfunction.
2. To diagnose the cause of system malfunction to a module level with a low probability of a false module pull, and
3. To measure and record module elapsed power-on time.

The importance of these objectives and their impact on the recommended BIT approach for MCF will become evident in later sections of this report.

1.2 Scope

The scope of this study includes the identification and evaluation of a recommended built-in-test approach for the AN/UYK-41(V) member of the Military Computer Family.* The study scope encompasses the conceptualization of an on-line maintenance approach for MCF and a detailed understanding of BIT techniques particularly suited to the AN/UYK-41(V) member and its constituent chassis and modules. Included in the proposed BIT approach is the identification and assessment of suitable on-line and idle time test techniques which are compatible with system level fault diagnostics and user interfaces. The present study results will be used as the technical basis for modifying the AN/UYK-41(V) form, fit and function specifications to insure the incorporation of the recommended BIT approach. This study does not include consideration of fault tolerant design approaches but rather addresses the issues specifically related to fault detection isolation and repair through module replacement.

1.3 Study Approach

The approach taken in this study was as follows:

1. Review AN/UYK-41(V) form, fit and function specifications. Review previous module, chassis and system level BIT approaches.
2. Based on BIT cost/performance guidelines supplied by the MCF/BIT selection committee working group, select candidate BIT approaches for the detection and identification of failed modules.

---

*The AN/UYK-41(V) and AN/GYQ-21(V) nomenclatures will be used interchangeably throughout this report. Both refer to the MCF version of the PDP-11/70.

3. Present descriptions of the candidate BIT approaches to the MCF/BIT selection committee.
4. Determine relative cost/performance of the candidate BIT approaches. Identify areas where the target BIT performance criteria can be modified to result in improved BIT performance and/or lower BIT cost.
5. Select a recommended BIT approach for the MCF computer system AN/UYK-41(V).
6. Present the recommended approach and supporting rationale to the MCF/BIT selection committee for evaluation.

An essential part of the present study was to understand the results of previous related studies. In particular, it was necessary to review the AN/UYK-41(V) form, fit and function specifications to understand the alternatives and limitations for BIT in this member of the Military Computer Family. At the same time, documentation on computers similar to the AN/UYK-41(V) was reviewed. Obviously, the DEC PDP-11/70 was of major interest because of the software and architectual similarities. Also, the AN/AYK-14(V) was relevant for two reasons, namely, the AN/UYK-41(V) and AN/AYK-14(V) bus similarities.

Also of interest were machines with extensive on-line fault detection, localization and, in some instances, recovery capabilities. The following machines in this category were considered:

1. Self-Testing and Repairing (STAR) Computer [5]
2. Bell System 1A Processor (No. 4 ESS) [6]
3. DEC PDP-11/60 [7]

Information on these machines were reviewed in order to maximize the transfer of useful fault detection and isolation features to the new generation machine.

In order to facilitate the objective evaluation of candidate built-in-test approaches, it was essential that a set of BIT evaluation parameters be established to serve as a basis upon which to select candidate BIT approaches.

3. Present descriptions of the candidate BIT approaches to the MCF/BIT selection committee.
4. Determine relative cost/performance of the candidate BIT approaches. Identify areas where the target BIT performance criteria can be modified to result in improved BIT performance and/or lower BIT cost.
5. Select a recommended BIT approach for the MCF computer system AN/UYK-41(V).
6. Present the recommended approach and supporting rationale to the MCF/BIT selection committee for evaluation.

An essential part of the present study was to understand the results of previous related studies. In particular, it was necessary to review the AN/UYK-41(V) form, fit and function specifications to understand the alternatives and limitations for BIT in this member of the Military Computer Family. At the same time, documentation on computers similar to the AN/UYK-41(V) was reviewed. Obviously, the DEC PDP-11/70 was of major interest because of the software architectual similarities. Also, the AN/AYK-14(V) was relevant for two reasons, namely, the AN/UYK-41(V) and AN/AYK-14(V) bus similarities.

Also of interest were machines with extensive on-line fault detection, localization and, in some instances, recovery capabilities. The following machines in this category were considered:

1. Self-Testing and Repairing (STAR) Computer-JPL [5]
2. Bell System 1A Processor (No. 4 ESS) [6]
3. DEC PDP-11/60 [7]

Information on these machines were reviewed in order to maximize the transfer of useful fault detection and isolation features to the new generation machine.

In order to facilitate the objective evaluation of candidate built-in-test approaches, it was essential that a set of BIT evaluation parameters be established to serve as a basis upon which to select candidate BIT approaches.

Obviously the impact of candidate BIT approaches on MCF hardware and software design time must be considered. For purposes of this study it will be assumed that, unless otherwise noted, these cost factors are proportional to the percentage increase in hardware and software required to support the recommended BIT approach.

The study approach called for the identification of cost/performance guidelines followed by the selection of candidate BIT approaches. The selection of candidate BIT approaches was based, in part, on the analysis which depicts where failures are most likely to occur in computers with architectures similar to the AN/UYK-41(V). An important consideration in this study in addition to fault detection was fault communication alternatives for different BIT approaches including redundancy in the fault reporting process.

Based upon all of these factors, candidate approaches were rank-ordered and a particular approach selected. The recommended BIT approach for MCF is discussed in detail in the following sections of this report.

1.4 Report Organization

The organization of this report reflects the study methodology in that background information about MCF in general and the MCF-AN/UYK-41(V) in particular, is presented in Sections 1.0 and 2.0. Section 1.0 reviews the general goals and objectives of MCF as they relate to built-in-test. Section 2.0 provides an in-depth description of the AN/UYK-41(V) including system specifications and physical characteristics. The remaining portion of Section 2.0 discusses the MCF two-level maintenance concept and its impact on BIT. Included in this section is a discussion of the assumed MCF fault population, BIT performance and cost measures of interest.

Section 3.0 presents a review of related prior generation computer fault detection and isolation approaches. Because of the special relationship of the MCF-AN/UYK-41(V) to the Digital Equipment Corporation PDP-11/70, it is important to understand DEC's hardware and software maintenance approach. By the same token, it is important to understand the built-in-test incorporated in the AN/AYK-14(V) because of the similarity in

the AN/UYK-41(V) and the AN/AYK-14(V) bus structures. Two fault tolerant computers were reviewed to ascertain the relevance of their fault detection rational to MCF. Finally, the relatively recently introduced DEC PDP-11/60 maintenance approach was considered because of its architectural similarities to the PDP-11/70 and its provisions for self-test through the plug-in Diagnostic Control Store (DCS) board.

Section 4.0 provides the overall framework for distributing BIT resources throughout the MCF AN/UYK-41(V). Included also is a description of fault reporting requirements with appropriate user interfaces.

In order to provide a quantitative basis for allocating BIT resources in the MCF-AN/UYK-41(V), a failure rate analysis of the PDP-11/70 was made. The results of this analysis is described in Section 5.0. Conclusions concerning where failures are most likely to occur are made based upon this analysis as well as other similar machines.

Section 6.0 contains specific recommendations for BIT at the module level. Included are recommendations for analog, memory, CPU, and I/O modules plus preliminary recommended approaches for testing the AN/UYK-41 (V) BUS.

Section 7.0 discusses the module/chassis elapsed time measurement problem. Two distinct approaches for determining elapsed time are presented.

In Section 8.0 an analysis of the performance and cost measures is done to evaluate the effectiveness of the built-in-test recommended in Sections 4.0 and 6.0.

Section 9.0 concludes the report with a summary and specific recommendations for further study. This section identifies areas where additional work is needed.

2.0 GENERAL SYSTEM DESCRIPTION AND BUILT-IN-TEST CONSIDERATIONS FOR THE MCF AN/UYK-41(V) COMPUTER SYSTEM

2.1 MCF AN/UYK-41(V) System Description

2.1.1 Summary of the System Specifications

The Form, Fit, and Function (F^3) Specification for the MCF AN/UYK-41(V) [AN/GYQ-21(V)] computer system have been specified by ITEK Corporation. The chart in Figure 2.1 describes the structure of the various ITEK documents which will be referenced throughout this report.

The AN/UYK-41(V) is a modular computer system which may be configured in various ways to meet the requirements of a large number of applications. There are basically two types of systems possible. A single processor system and a dual processor system. The characteristics of these two types of systems are given in the Tables 2.1 and 2.2, respectively.

The architecture and the instruction set of the AN/UYK-41(V) have been designed such that it may be used to emulate the Digital Equipment Corporation's PDP-11/70 computer.

2.1.2 System Configuration

The AN/UYK-41(V) computer system(s) consists of multiple chassis. The single processor system consists of one Main Computer Chassis No. 1, one Memory Expansion Chassis, and one I/O Expansion Chassis as shown in the Figure 2.2. The dual processor system consists of one Main Computer Chassis No. 2, two Memory Expansion Chassis, and two I/O Expansion Chassis as shown in the Figure 2.3.

These chassis are interconnected via interface cables and mounted in rack assembly or other suitable structure per system application requirements.

The hardware for the entire system is partitioned into pluggable modules. These modules are then used as standard building blocks to configure functionally large or small computers depending upon the application. The types of standard modules available for the AN/UYK-41(V) computer system are listed in Table 2.3 along with a brief description of their functions.

Each chassis within an AN/UYK-41(V) computer system will carry its own power supply for all modules contained therein. Each chassis will also

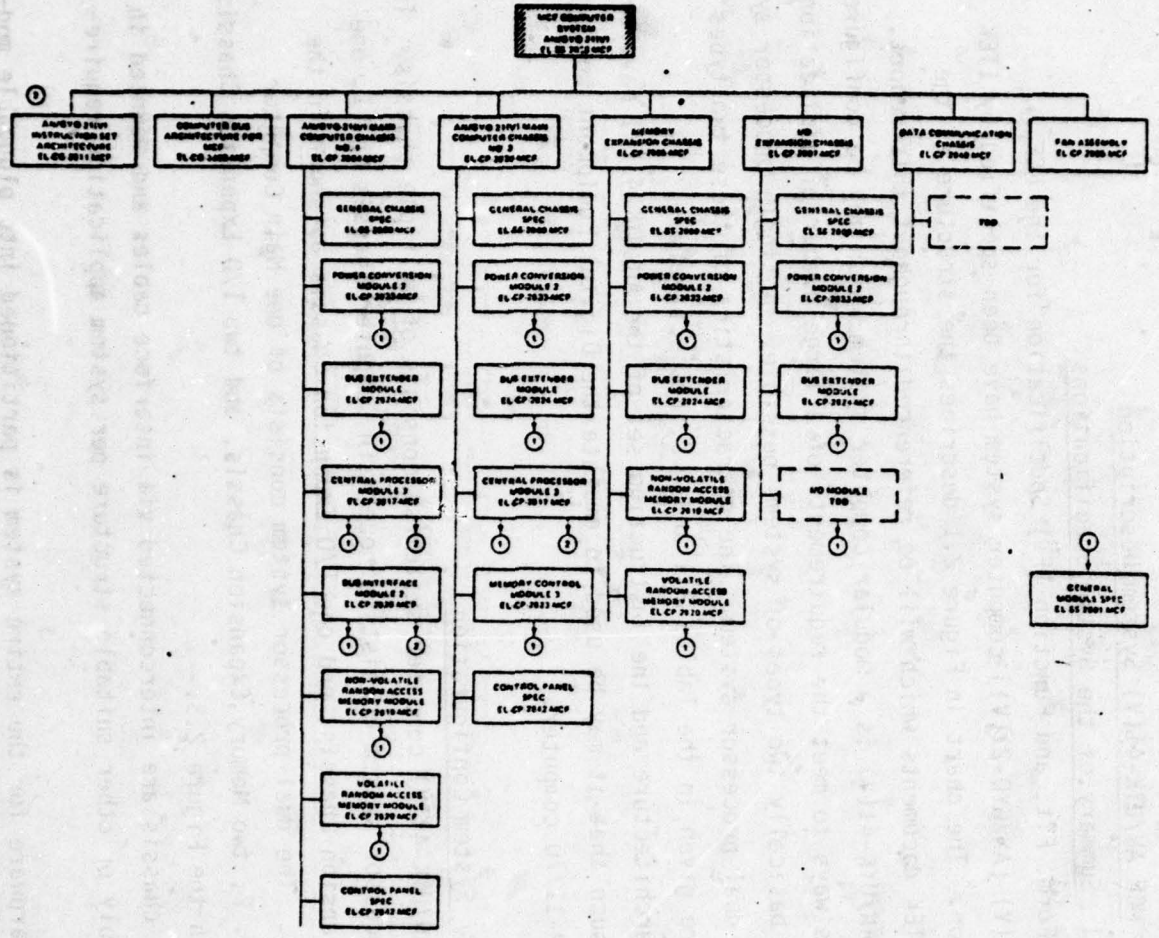


Figure 2.1. MCF Computer System AN/GYQ-21(V) Form, Fit, and Function Specification Structure [8]

TABLE 2.1. MCF AN/GYQ-21(V) SINGLE PROCESSOR COMPUTER SYSTEMS CHARACTERISTICS [8]

System Parameters	Configuration		
	Minimum System	Maximum System	Typical System
Size	1, type III chassis	17, type III chassis	3, type III chassis
Weight (excluding cables)	80 pounds max	1360 pounds max	240 pounds max
Power dissipation (excluding I/O expand chassis, data comm chassis and fan(s))	• 500 w max - option 1* • 485 w max - option 2*	• 2200 w max - option 1 • 2850 w max - option 2	• 930 w max - option 1 • 960 w max - option 2
Memory capacity	64K words	2000K words	256K words
I/O capacity	• 4 MCF I/O chan • UNIBUS®	• 84 MCF I/O chan • UNIBUS® • 32 data comm channels	• 4 MCF I/O chan • UNIBUS® • 16 data comm channels
Instruction execution throughput	• 550 KOPS min - option 1 • 700 KOPS min - option 2	• 550 KOPS min - option 1 • 700 KOPS min - option 2	• 550 KOPS min - option 1 • 700 KOPS min - option 2
Reliability (excluding I/O expand chassis, data comm chassis and fan(s))	• 1800 hrs min - option 1 • 1600 hrs min - option 2	• 240 hrs min - option 1 • 180 hrs min - option 2	• 875 hrs min - option 1 • 700 hrs min - option 2

* Option 1 - non-volatile main memory
Option 2 - volatile main memory

®UNIBUS is a registered trademark of the Digital Equipment Corporation, Maynard, Massachusetts

TABLE 2.2. MCF AN/GYQ-21(V) DUAL PROCESSOR COMPUTER SYSTEMS CHARACTERISTICS [8]

System Parameters	Configuration		
	Minimum System	Maximum System	Typical System
Size	5, type III chassis	33, type III chassis	7, type III chassis
Weight (excluding cables)	400 pounds max	2640 pounds max	560 pounds max
Power dissipation (excluding I/O expand chassis, data comm chassis, and fan(s))	• 1530 w max - option 1* • 1540 w max - option 2*	• 4000 w max - option 1 • 5250 w max - option 2	• 1530 w max - option 1 • 1540 w max - option 2
Memory capacity	128K words	4000K words	784K words
I/O capacity	• 20 MCF I/O chan • 2 UNIBUS®	• 160 MCF I/O chan • 16 UNIBUS® • 64 data comm channels	• 20 MCF I/O chan • 2 UNIBUS® • 32 data comm channels
Instruction execution throughput	• 1000 KOPS min - option 1 • 1200 KOPS min - option 2	• 1000 KOPS min - option 1 • 1200 KOPS min - option 2	• 1000 KOPS min - option 1 • 1200 KOPS min - option 2
Reliability (excluding I/O expand chassis, data comm chassis, and fan(s))	• 540 hrs min - option 1 • 440 hrs min - option 2	• 130 hrs min - option 1 • 100 hrs min - option 2	• 540 hrs min - option 1 • 440 hrs min - option 2

* Option 1 - Non-volatile main memory
Option 2 - volatile main memory

®UNIBUS is a registered trademark of the Digital Equipment Corporation, Maynard, Massachusetts

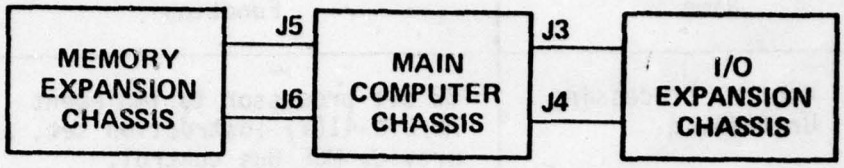


Figure 2.2. AN/GYQ-21(V) Main Computer Chassis No. 1 Expansion Capability [9]

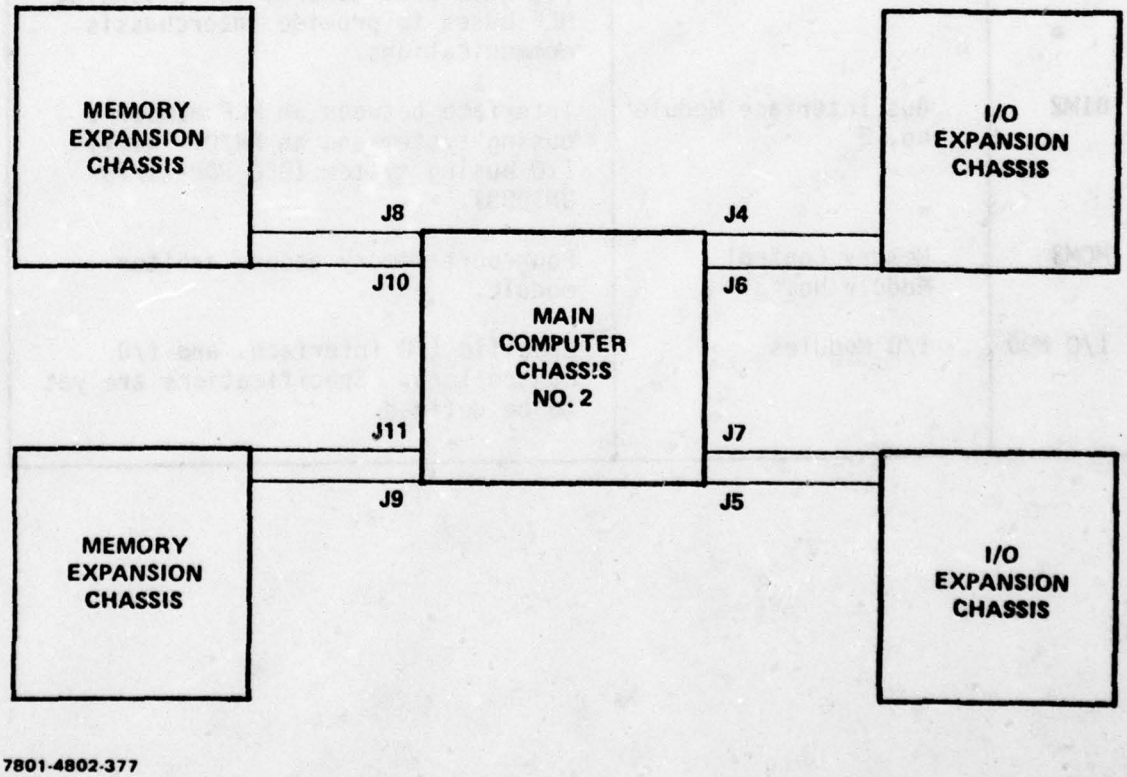


Figure 2.3. AN/GYQ-21(V) Main Computer Chassis No. 2 Expansion Capability [10]

TABLE 2.3. MCF AN/UYK-41(V) HARDWARE

Module	Name	Function
CPU3	Central Processing Unit No. 3	32 bit processor to implement AN/UYK-41(V) instruction set, and provide MCF Bus control.
NRAM	Non-volatile Random Access Memory	32K or 64K words of non-volatile, random access, read/write memory.
VRAM	Volatile Random Access Memory	32K or 64K words of volatile random access, read/write memory.
PCM2	Power Conversion Module No. 2	Regulated dc power supplies operating from single phase ac power to provide +5V, -12V, and +15V outputs.
BEM	Bus Extender Module	Interface drivers/receivers with bidirectional control for extending MCF buses to provide interchassis communications.
BIM2	Bus Interface Module No. 2	Interface between an MCF member's busing system and an AN/UYK-41(V) I/O busing system (DEC PDP-11/70 UNIBUS).
MCM3	Memory Control Module No. 3	Four-port memory access arbiter module.
I/O MOD	I/O Modules	Specific I/O interfaces and I/O controllers. Specifications are yet to be defined.

contain the appropriate backplane connectors for the modules to be plugged in that chassis. The typical complement of modules to be used with the Main Computer Chassis 1 and 2, the Memory Expansion Chassis and the I/O Expansion Chassis are shown in Figure 2.4, 2.5, 2.6, and 2.7, respectively.

2.1.3 Physical Characteristics

All chassis will exist in one of three configurations (Type I, II and III), each having the same cross-section and varying in length depending on functional complexity and growth provisions. The standard dimensions are: height 7.62 inches, width 10.12 inches, and length 12.56 or 15.56 or 19.56 inches. Each chassis will provide mechanical support and cooling to the MCF modules. Cooling provisions include externally supplied cooling air directed through plenums and/or conduction to auxiliary heat exchangers. Each chassis consists of an enclosure, backplane interconnect and input/output connectors as defined by the specific chassis requirements.

The modules are the lowest level replaceable units of the Military Computer Family. All modules will have the same cross-section (height 6.0 inches, width 9.0 inches) and will vary in depth depending on the functional complexity (standard depths 0.5, 1.0, 1.5, 3.0, 3.5 or 5.0 inches). All modules are conduction cooled and all modules except the power supply modules, employ NAFI type connectors (76, 152, or 304 pins) for electrical interface with the chassis.

2.2 Reliability and Maintainability of MCF Computer Systems

2.2.1 Environment

The MCF computer systems are expected to operate reliably under a wide range of environmental conditions. The details of environmental specifications under operating and non-operating conditions for the chassis, as well as the modules, are given in the ITEK specifications [13], [14]. These include mechanical, electrical and thermal specifications. These environmental conditions have been considered when performing reliability calculations as stated below.

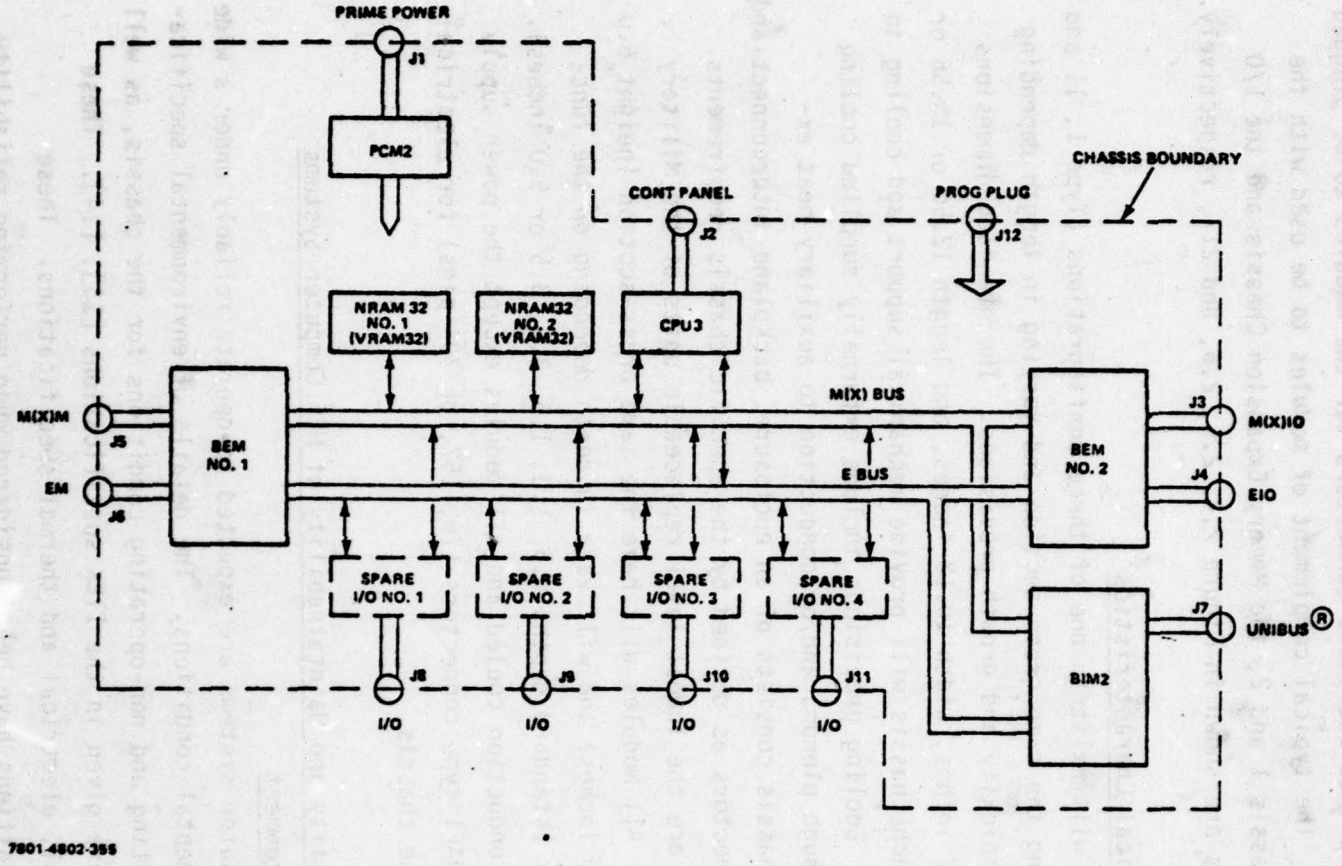


Figure 2.4. AN/GYQ-21(V) Main Computer Chassis No. 1 [9]

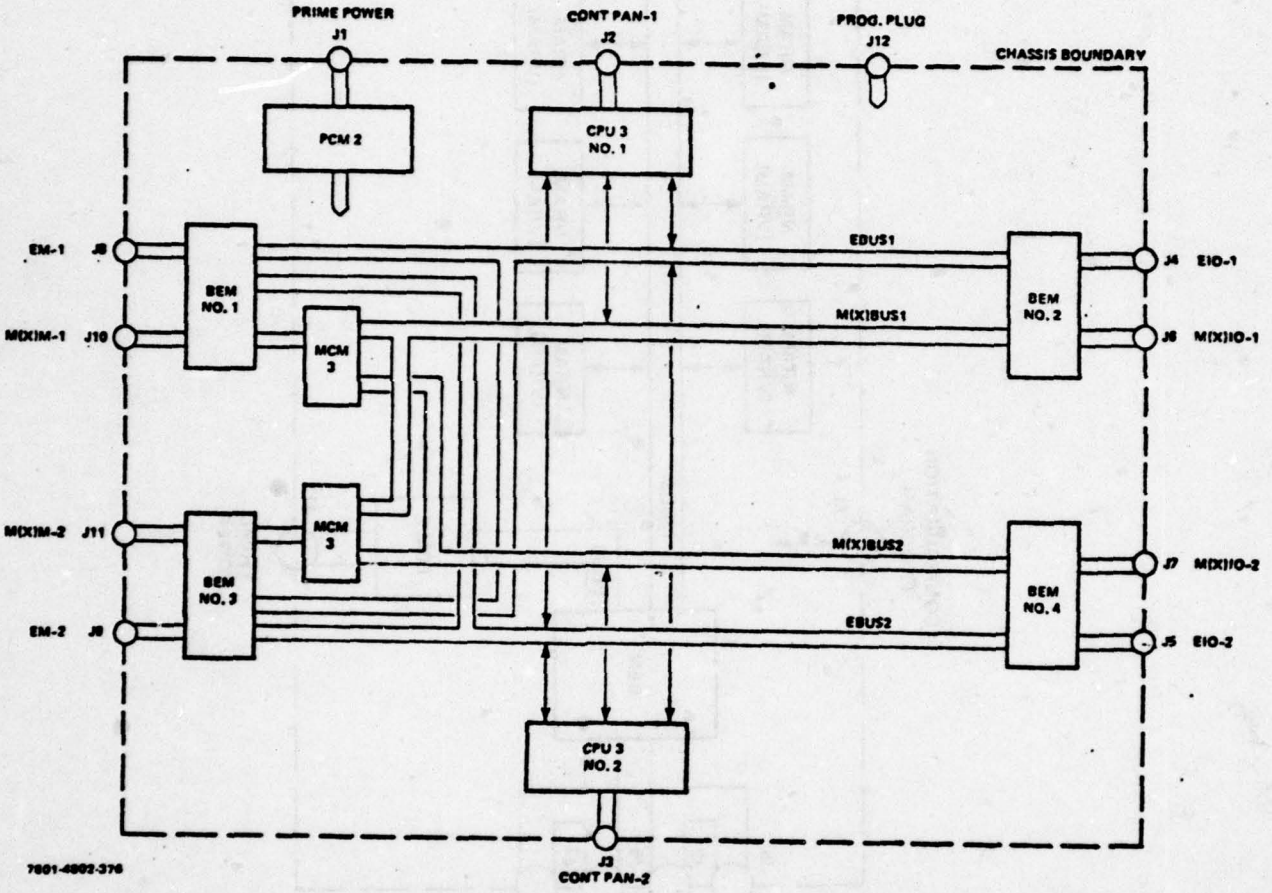


Figure 2.5. AN/GYQ-21(V) Main Computer Chassis No. 2 [10]

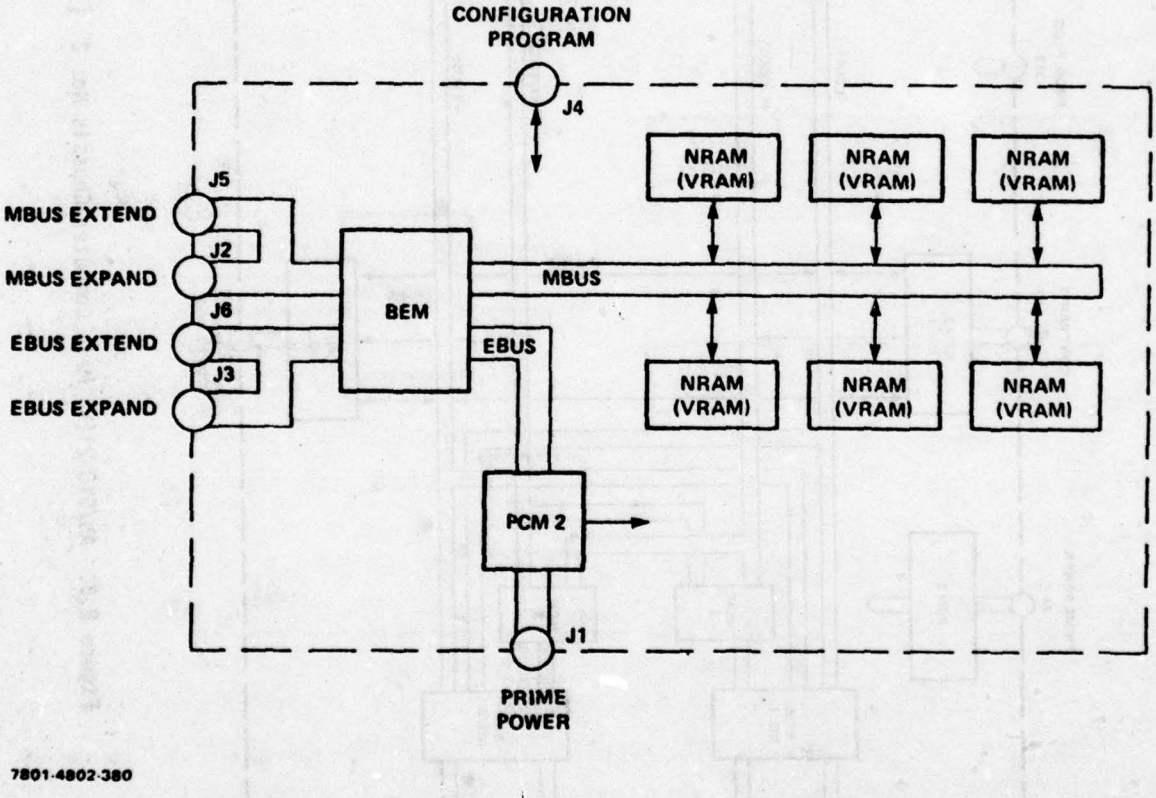


Figure 2.6. Memory Expansion Chassis Block Diagram [11]

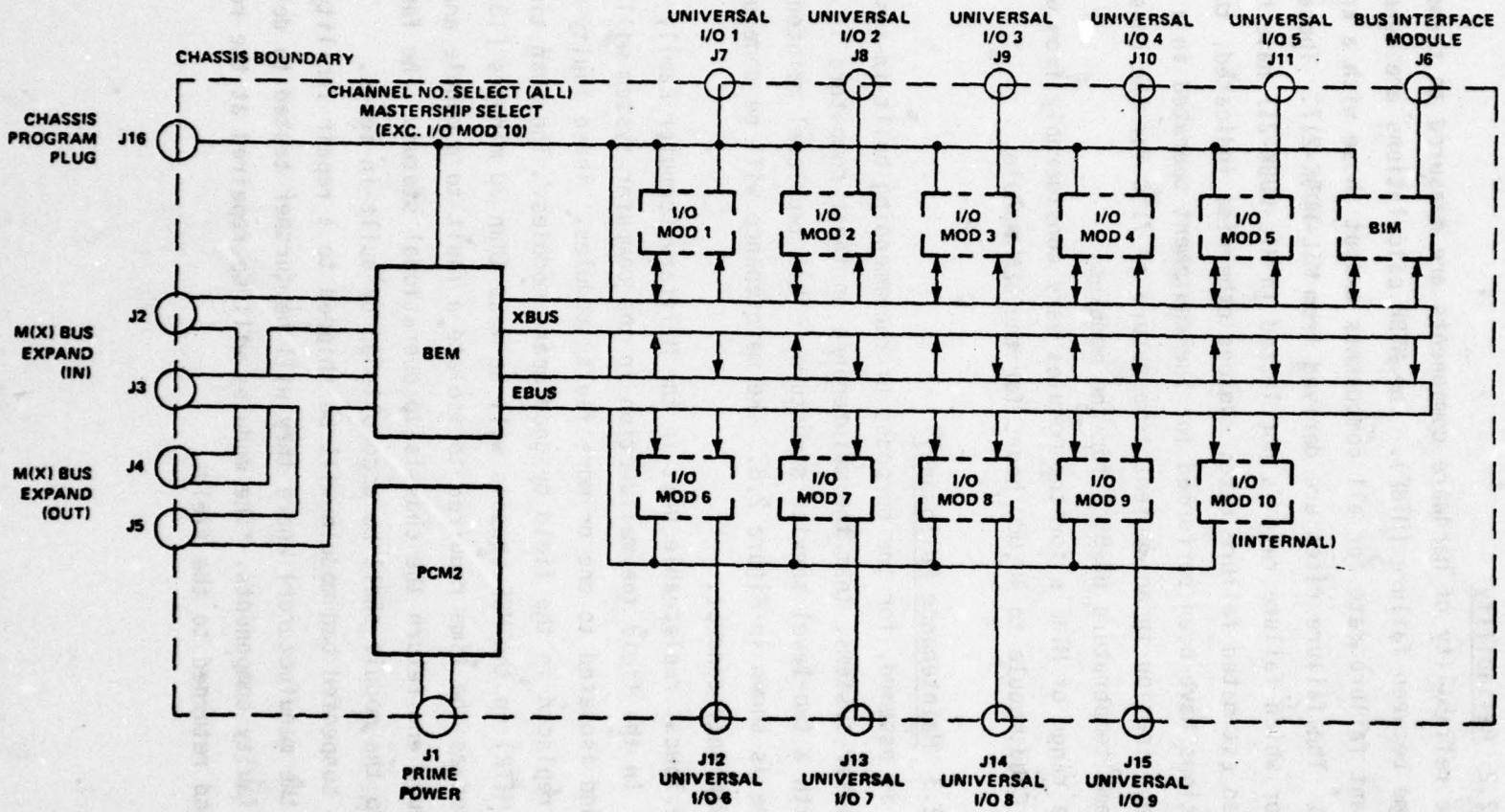


Figure 2.7. I/O Expansion Chassis Block Diagram [12]

2.2.2 Reliability

The reliability of hardware components are measured in terms of the mean time between failure (MTBF). The MTBF calculations are done assuming a constant failure rate for all components except those with a known limited life. The failure rates are derived from MIL-HDBK-217. Those components for which failure rate is not listed in MIL-HDBK-217 have been assigned an estimated failure rate. Unless otherwise indicated, the MTBF calculations have been performed for the equipment operated in a mobile ground application in an ambient temperature of 71°C for the chassis and a ramp clamp temperature of 85°C for the modules.

The range of MTBF's for the modules vary considerably from 6,000 hours for the CPU3 module to 40,000 hours for the BEM module.

2.2.3 Maintenance Philosophy

It is assumed, for the purposes of recommending built-in-test for the MCF computer systems, that the maintenance on these computers is to be provided with a two-level service structure. This two-level maintenance structure is shown in Figure 2.8. The maintenance will be done under a module warranty concept.

The lowest replaceable unit in the Military Computer Family is the module. In the field the malfunction in the computer system will be detected and isolated to one or more faulty modules. These faulty modules will be replaced in the field by good spare modules. The mean time to repair (MTTR) on the MCF chassis will be less than 30 minutes [13]. MTTR is defined as the time required to isolate a fault to a module and replace that module and return the chassis to operational status. The fault isolation to the module shall be accomplished by built-in-tests.

The suspected bad module will be shipped to a repair facility (perhaps that of the manufacturer) where they will be further tested to detect and isolate faulty components. The modules will be repaired at the repair facility and returned to the field.

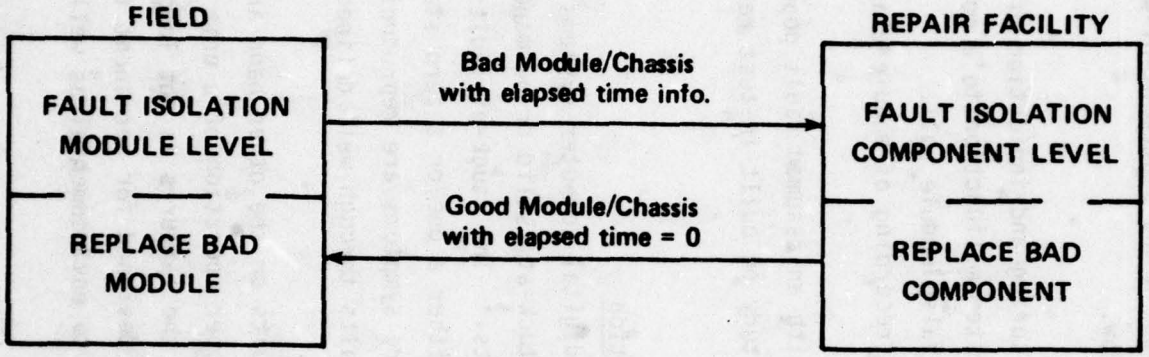


Figure 2.8. Two-Level MCF Maintenance Philosophy

2.3 Built-In-Test Considerations

2.3.1 Overall Built-In-Test Objectives

In order to accomplish the reliability and maintainability goals for the MCF computer systems, certain general objectives as discussed in Section 1.1 were set forth in the statement-of-work for this study. They are briefly restated below.

1. Continuous monitoring and indication of system malfunction.
2. Diagnosis of system malfunction to a module level with a low probability of false module pull.
3. Measurement and recording of module elapsed power-on time.

These objectives along with an assumed fault population serve as the guidelines for the detailed study on built-in-test requirements for the MCF computer systems.

2.3.2 Fault Population

Hardware faults in digital computer systems can be classified in two basic categories. The stuck-at (solid or permanent) faults and the intermittent (transient) faults.* The stuck-at faults occur when a logic signal remains permanently in either a one or a zero state. Such failures are consistent and the failure symptoms are reproducible. This facilitates the isolation of stuck-at faults through well defined diagnostic test procedures.

The intermittent faults on the other hand are defined as random failures that prevent the proper operation of a unit for a short period implying that the duration of the failures is not long enough for the application of a test procedure designed for permanent faults [15]. The intermittent faults occur due to environmental as well as non-environmental

---

*Definitions of commonly used fault detection, isolation, and repair terms may be found in Appendix A of this report.

reasons. Environmental conditions such as temperature, humidity, vibration, electrical and electromagnetic interferences, etc., induce intermittent faults. More important, however, are the non-environmental intermittent faults which are caused by loose connections, resistance variations, deteriorating or aging components, etc.

Recent studies in fault diagnosis [15], [16], [17] indicate that a major portion of digital system malfunctions are caused by intermittent faults. In some systems, 80 to 90 percent of the faults are estimated to be intermittent [15]. Furthermore, these faults have been found to account for more than 90 percent of the total maintenance expense because they are difficult to detect and isolate.

2.3.3 Built-In-Test Functions

There are several functions that the built-in-tests must perform with the ultimate objective of enhancing the maintainability of the MCF computer system. These functions are listed below.

1. Fault Detection
2. Fault Isolation
3. Fault Indication
4. Fault Communication (Reporting)
5. Fault Logging
6. Fault Characterization (stuck-at, transient)
7. Fault Handling (Error Recovery)

The above mentioned built-in-test functions are usually implemented in hardware (including firmware) and in software. The primary objective is the fault detection and isolation. These two objectives may be accomplished in various ways: on-line (using either continuous monitoring or by periodic sampling), during idle time, and off-line. The definitions of these terms can be found in the Appendix A.

Fault indication implies some form of audio-visual cue to the operator. This indication may be in terms of indicator lights or alpha-numeric

displays, or printed message regarding the status of the system. If the system becomes non-operational, then sufficient fault isolation information should be available to the operator to enable a repair.

The fault communication, logging and characterization are also essential functions which provide a means for establishing the health status of the computer system at any given time. These aid in fault diagnosis and ultimately in automatic error recovery if possible. Faults detected at the lowest level (module level) should be communicated to the higher levels (chassis, system levels). Fault communication may be done via regular data paths in the system or via separate fault communication channels.

Fault logging implies any means of keeping a detailed record of the failures as they occur. Such error record provides a diagnostic feedback and is necessary to characterize the types of faults that occur most frequently. This is particularly useful in diagnosing failures due to transient or intermittent faults. Since the failure symptoms due to intermittent faults are not easily reproducible, the isolation of intermittent faults relies more on the accumulated error statistics. Isolation of an intermittent fault becomes easier if it can be mapped to a set of intermittent faults which can be probabilistically related to known sources of failures.

Once a fault has been detected while the computer is executing a certain instruction of the application program, several responses are possible which depend on the type of fault, the machine status at the time the fault occurred, the recovery features designed in the computer architecture. All of these responses to a failure may be broadly classified under fault handling. Typically, one of the following actions occur when a fault is detected.

1. Abort current instruction and halt.
2. Branch control immediately to diagnostic hardware, firmware or software for fault diagnosis.
3. Attempt instruction retry.

Although fault handling is an essential function of the built-in-test, it is considered to be beyond the scope of this report. Therefore, it will not be treated in any greater detail. Emphasis will be placed on the detection and identification of the failed modules.

2.3.4 Built-In-Test Approaches

In view of the built-in-test objectives stated in Section 1.1 and the Form, Fit, and Function (F^3) specifications summarized in Section 2.1, a top-down approach to the selection of candidate BIT techniques is recommended. In the Military Computer Family, the following hierarchical levels are easily identifiable.

1. MCF Member Level (System Level)
2. Chassis Level
3. Module Level

Built-In-Test techniques which will be considered may be incorporated at any one or combinations of the above mentioned hierarchical levels. The basic approach used in this study is to identify a set of BIT techniques at each level and then select candidate BIT techniques based on certain performance versus cost criteria. The BIT effectiveness criteria for performance and cost are discussed in the next section.

Each hierarchical level affords a certain level of fault detection and a degree of fault isolation capability because of the observability and controllability problems. In order to enhance the performance/cost figure of the candidate BIT techniques, it is necessary to study the fault detection requirements and the BIT resources available at each hierarchical level. Furthermore, the fault communication and hardware/software interfaces between the various constituent BIT elements at each hierarchical level need to be investigated.

In summary, fault detection and identification at the various levels may be performed using continuous monitoring, sampled monitoring, idle time monitoring or other off-line techniques. Approaches will be emphasized

which will provide continuous monitoring with minimum impact on system performance.

2.3.5 Built-In-Test Effectiveness Criteria for Performance and Cost

The effectiveness of any built-in-test approach may be measured in terms of the ratio of its performance to the cost of implementing it. In quantifying the performance/cost ratio there are a significant number of parameters or sets of parameters which can be considered.

In view of the broad objectives of the built-in-tests for the MCF computer systems, a set of general parameters has been chosen. Since the main objective of the BIT for the MCF is to detect and isolate faults with a low probability of false module pull, the performance parameters should be able to measure the probabilities of detecting and localizing faults as well as the probabilities of false alarms. Furthermore, since the mean time to repair is also an essential consideration in the maintenance of MCF computer systems, the performance parameters should include the time required to detect and isolate faults. This forms a set of five performance measurement parameters which are defined below.

P_{SFD} - Probability of System Fault Detection

P_{LFE} - Probability of Localizing to Faulty Element

P_{FA} - Probability that suspected Faulty Element is not Faulty. (False Alarm)

T_{SFD} - Time to System Fault Detection

T_{LFE} - Time to Localize to Faulty Element

The cost of implementing a BIT approach can be broadly categorized into hardware and software costs. The hardware costs mainly involve space (A), power (P), and failure rate (FR). The hardware cost can be measured in terms of the percent increase in the space, power, and failure rate due to the additional BIT circuitry.

The software costs on the other hand are more difficult to assess. The software is impacted at three levels: 1) operating system software

(OS), 2) applications software (AS), and 3) diagnostic software (DS). Additional BIT functions typically increases the operating system responsibilities because it must provide for the user/BIT interface and may have to perform error handling tasks. The BIT functions are generally transparent to the user. However, the application software will be impacted if the user is to be provided with the option to control some of the BIT functions. The diagnostic software can generally be simplified by additional BIT hardware.

The Figure 2.9 and the Table 2.4 summarize the effectiveness criteria used in accessing the BIT approaches for the MCF computer systems.

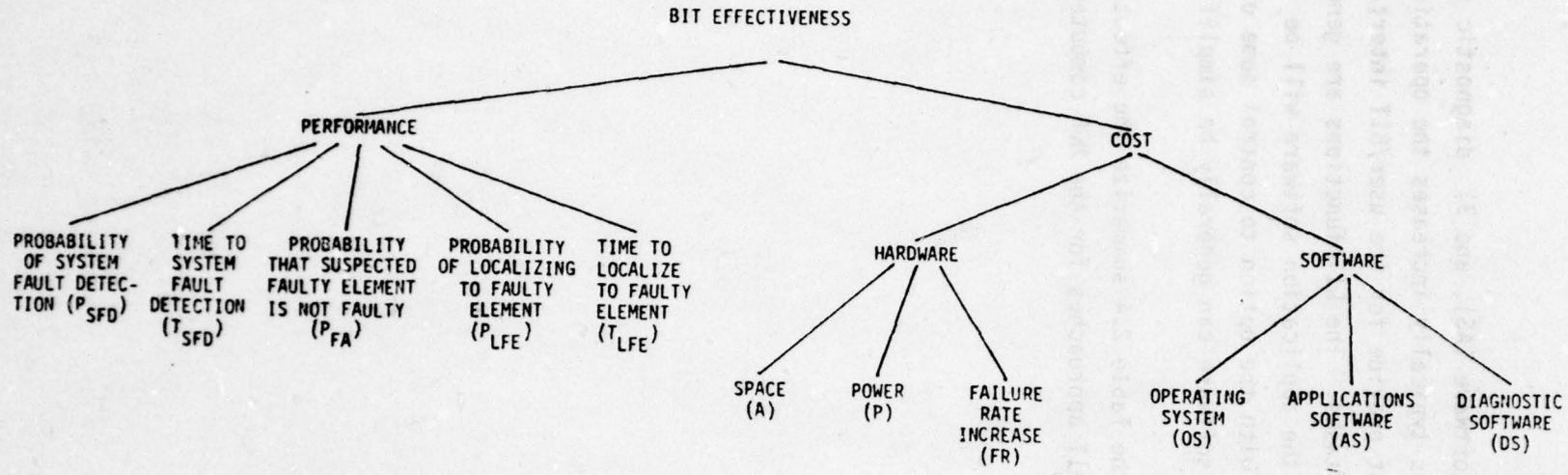


Figure 2.9 Built-In-Test Effectiveness Criteria Used in Assessing BIT Approaches For MCF

TABLE 2.4. MCF BUILT-IN-TEST PERFORMANCE/COST CRITERIA

Performance

Criteria	Comment
1. Probability of on-line detection of a system malfunction (P_{SFD})	Implies fault detection and notification of fault.
2. Time to detection of system malfunction (T_{SFD})	Includes fault detection error latency plus user notification time.
3. Probability that a suspected faulty element is not faulty (P_{FA})	Refers to maintenance false alarm rate.
4. Time to localize to a faulty system element (T_{LFE})	Time between user initial notification that system has malfunctioned and when user determines which element is faulty.
5. Probability of localizing to a faulty system element (P_{LFE})	Probability of determining which module, chassis, member is faulty.

Cost

Criteria	Comment
Space (A)	Includes board space, chassis slots, module pinouts, chip count, etc.
Power (P)	Refers to additional power required by BIT circuitry.
Failure Rate Increase (FR)	Reduction in module, chassis and/or system MTBF due to BIT circuitry.
Operating System (OS)	May be impacted if error handling is part of the OS responsibility. Also can be impacted by user/BIT interface.
Applications Software (AS)	May be impacted if user is provided with the option to control some of the BIT functions.
Diagnostic Software (DS)	Generally can be simplified by BIT

3.0 OVERVIEW OF SOME RELATED PRIOR GENERATION COMPUTER BUILT-IN-TEST FEATURES

In an effort to build on the BIT knowledge and experience that other people have developed, a review of prior computers was carried out. Careful attention was paid to BIT techniques, not only in fault detection schemes, but in error handling and fault reporting approaches also. Some of these computers have fault tolerant features built into them that affect their maintainability. Special note was made of these features when they might be applicable to the MCF computer systems. Five computers were selected for this detailed fault detection/reporting study. The STAR computer and 1A Processor (from the No.4 ESS) were chosen because of their extensive fault tolerant features. The PDP 11/60 and 11/70 were included in this group as representatives of current commercial minicomputers. The last computer in this group is the AN/AYK-14(V) which represents a modern military minicomputer.

3.1 STAR

The Jet Propulsion Laboratory developed the STAR computer to be used in space missions where on-site repair was impossible. Therefore, it was necessary to design a computer that was ultra-reliable. Toward this goal, fault-tolerance was used extensively. While the MCF computers will not be designed for complete fault tolerance, many of the fault detection techniques used in the STAR's fault tolerance can be used.

In the STAR computer, all machine words, both data and instructions, are encoded in error-detecting codes. Fault detection occurs concurrently with the execution of the programs. The error-detecting codes are supplemented by monitoring circuits which serve to verify the proper synchronization and internal operations of the functional units. Each functional unit is autonomous and contains its own sequence generator, as well as storage for the current operation code, operands and results. One out of every ten clock cycles is used to report status (error) information to the central control unit. Status message originating circuits within the I/O, as well as the status lines are duplicated to allow the detection of a fault in the status message. The absence of an expected "Output Active"

message is also a fault condition. Finally, some more critical I/O units are duplicated to ensure that all operations are performed correctly.

3.2 1A Processor

The 1A Processor of the No. 4 ESS (Electronic Switching System) was developed by the Bell System to handle a large number of long distance telephone calls with an availability very close to 100%. In fact, the objective was less than two minutes a year down time. With reliability and availability goals this high, it is necessary to use fault tolerance techniques to allow operation of the unit until the failed part can be replaced. Special attention was given to the fault detection techniques as these are essential to BIT, also. A block diagram of this processor is shown in Figure 3.1.

In the 1A processor, all subsystems have redundant units that are connected to the basic system via a redundant bus system. The central control unit is fully duplicated; they operate in step and compare all results. The memory subsystem that contains the program consists of a prime set plus two "roving spare" units. In the event of a failure, the contents of the faulty memory is copied from the duplicate copy to one of roving spare units. The memory that stores the data on transient calls is fully duplicated on-line.

Parity checks are performed on all communications, that is on both address and data over all buses. Within subsystems, there are interval self checking timers that can detect major timing errors and lack of subsystem response. Each peripheral device is polled to determine its status. Under program control a signal can be sent to each I/O device to request an automatic response, which checks the I/O loops. All vital communications buses are duplicated and transmitted information contains redundant information for error detection. In addition, transformers are used to couple the bus to minimize the probability that a faulty I/O device could make the bus completely unusable for all other devices on the bus. Internal parity is carried with most of the information with each subsystem. Software as well as the normal hardware checks are used to check for parity errors, thus each verifying the proper operation of the others.

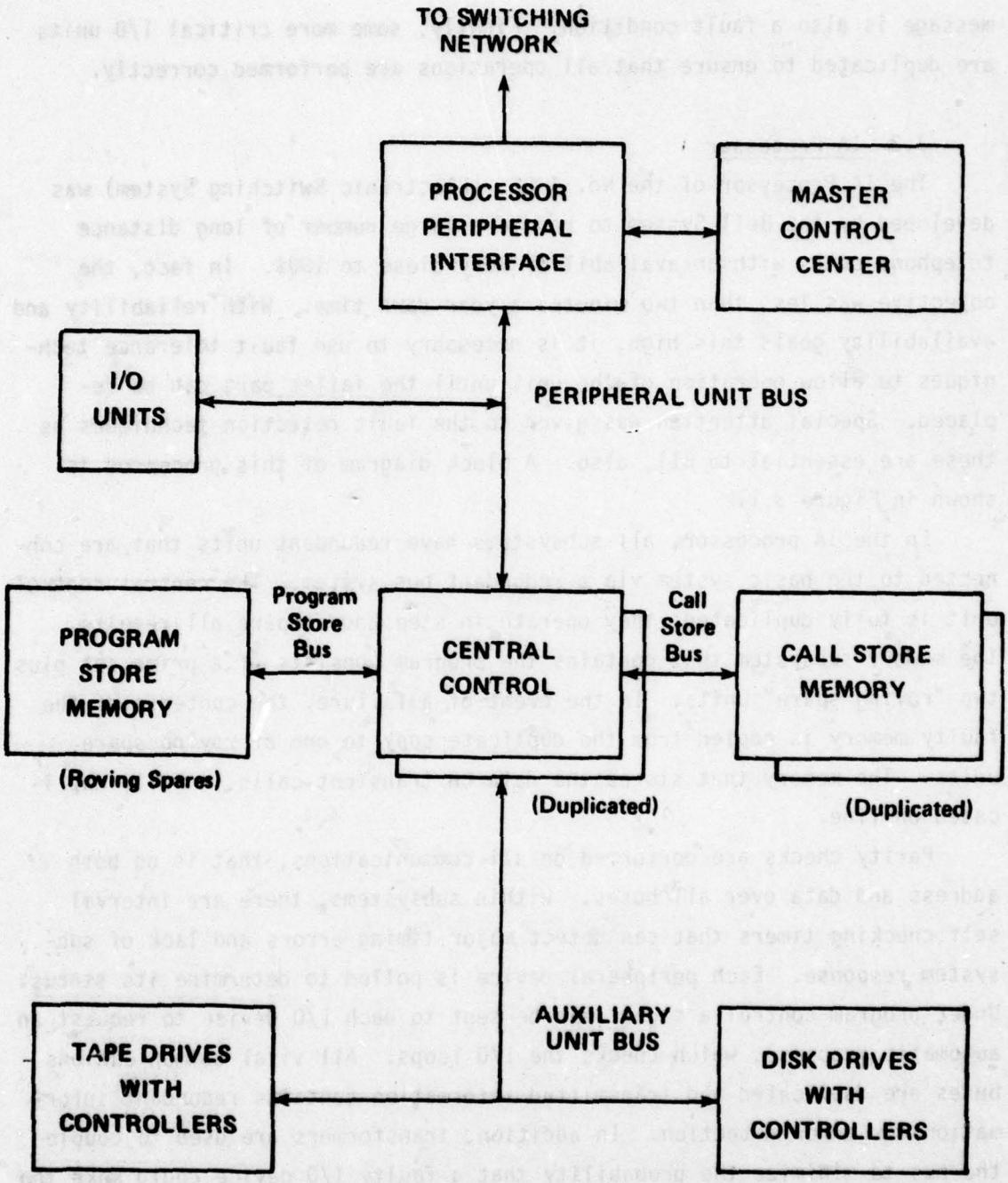


Figure 3.1. 1A Processor Block Diagram

3.3 PDP-11/60

The PDP-11/60 is a general purpose commercial minicomputer manufactured by the Digital Equipment Corporation (DEC) [7]. It is a 16-bit user microprogrammable machine. Several test and fault diagnosis features have been incorporated in the PDP-11/60 design that make it more easily maintainable. The PDP-11/60 features related to built-in-test are discussed below.

1. Diagnostic/Bootstrap Loader. The bootstrap loader program is stored in a special ROM along with a rudimentary diagnostic program. This diagnostic is executed each time the system is bootstrapped. It tests the central processor, cache memory, main memory and the basic PDP-11/60 instruction set. Hardware problems detected by the diagnostics cause the computer to halt and the fault signature is displayed on the console panel.
2. Diagnostic Control Store (DCS) Module. This module has a 2K x 48-bit ROM which contains microdiagnostics for testing the CPU. The module has its own self-testing diagnostic microcode. The microdiagnostics can be initiated from the console panel or the DCS module itself. LED's on the DCS module indicate an error code which can be looked up in a fault directory to determine the defective CPU board(s).
3. Error Logging. The CPU logs error information into special scratchpad registers at the time of error. This error log includes UNIBUS data, physical address, cache address, cache data, next microaddress, last interrupt vector at the time of error. This error log can be read from the console panel or used by diagnostic programs for fault isolation.
4. Parity bit(s) and associated parity generation/checking are available on cache and main memory (core). For semiconductor main memory (MOS) error correcting code (ECC) is also available optionally.
5. Software Diagnostics. There are several types of diagnostic software available for fault detection, isolation, and reliability tests. This software typically resides on mass storage devices and must be loaded in the main memory before being executed.

Table 3.1 summarizes the fault diagnosis features available on the PDP-11/60. It is interesting to note that even with the above described hardware diagnostic features, the PDP-11/60 system does rely heavily on off-line stand-alone diagnostic software for fault isolation.

3.4 PDP-11/70

The PDP-11/70 is an older but larger computer than the PDP-11/60 [19]. It is a 16-bit medium range general purpose computer. It has all of the fault detection and isolation features discussed above for the PDP-11/60 with the exception of the Diagnostic Control Store. Although PDP-11/70 is a microprogrammed machine, it is not user microprogrammable. Its initial design did not allow for expansion of the micromemory to incorporate microdiagnostics. However, this does not mean that microdiagnostics cannot be incorporated in the MCF-AN/UYK-41(V) which emulates the PDP-11/70 instruction set. Table 3.2 summarizes the fault detection and isolation features available on the PDP-11/70 computers.

In addition to the above discussed fault detection and isolation features, the PDP-11/70 and also PDP-11/60 have certain on-line fault reporting and subsequent error handling features. The following general philosophy is followed. The hardware faults are classified into soft errors and hard errors. All errors when detected are logged in error status registers. The soft errors are generally those that can be recovered. It is the responsibility of the system software or the application software to check the error bits in the error status registers to determine if a soft error has occurred and provide the necessary error handling. The hard errors on the other hand are not recoverable and cause a trap either midway through an instruction or upon completion of the current instruction. Each hard error or a group of hard errors causes a trap (vectored interrupt) via a predefined location in the memory. It is the responsibility of the system software to provide trap handling routines to diagnose the fault. In some cases, e.g., cache and memory management units, partial instruction retry is attempted before generating the trap. So, there is a combination of hardware/software to provide a limited amount of error correction and recovery. Such features of the PDP-11/70 are summarized in Table 3.3.

TABLE 3.1. PDP-11/60
FAULT DETECTION & ISOLATION FEATURES [18]

Monitored or Tested By: / System Component	CPU	Instruction Set	UNIBUS	Cache	Cache Addresses	Main Memory	Memory Management	Integral FP Instructions	FPU-F	UCS	Power Fail and Restart	Peripheral Controllers	Peripheral Subsystems	UNIBUS Devices	Remarks
Bootstrap Module (M9301-YH)	✓	✓	✓	✓		✓									Hardware
Parity Checks	✓			✓	✓	(1)				✓		✓			Hardware detected, but corrected by software
Error Detection/Correction				✓		✓									
Light Emitting Diodes (LEDs)	✓					✓						✓			Hardware
Error Logging Hardware	✓		✓	✓		✓	✓								Hardware
DEC X11 Subsystem Exerciser	✓					✓							✓		Software
Subsystem Diagnostics				✓		✓	✓	✓	✓					✓	Software
Stand-alone Diagnostics	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	Software, for F/S use only
User-Mode Diagnostics											✓	✓	✓	✓	Software, supported by IAS, RSX-11M,D
Diagnostic Control Store (DCS)	✓	✓	✓					✓			✓				Hardware Module

Legend (1) On Add, Data, and Control references to main memory
Note - DCS and the console have separate, dedicated diagnostics

TABLE 3.2. PDP-11/70 FAULT DETECTION & ISOLATION FEATURES [20]

Monitored or Tested by: \ System Component	CPU	Instruction Set	UNIBUS	UNIBUS Map	Cache	Cache Addresses	Main Memory	Memory Management	FPP	RH70 Massbus Controllers	Power Fail and Restart	Peripheral Controllers	Peripheral Subsystems	Massbus Devices	UNIBUS Devices	Remarks
Bootstrap Module (M9301-YC)	X				X		X									Hardware
Parity Checks	X			X	X	X	(1)			X		X				Hardware detected, but corrected by software
Error Detection/Correct					X		X									Same as above
Light Emitting Diodes (LEDs)	X						X					X				Hardware
Error Logging Hardware	X		X		X		X	X								Hardware
DEC/X11 Subsystem Exerciser	X						X						X			Software
Subsystem Diagnostics	X			X	X		X	X	X	X				X	X	Software
Stand-alone Diagnostics	X	X	X	X	X		X	X	X	X	X	X	X	X	X	Software, for F/S use only
User-Mode Diagnostics										X		X	X	X	X	Software, supported by IAS, RSX-11D

Legend: (1) On Add, Data, and Control references to main memory

Table 3.3 PDP-11/70 FAULT REPORTING & ERROR HANDLING FEATURES

	MEMORY: RAM	HARDWARE REDUNDANCY	CPU	I/O: UNIBUS	I/O: HIGH SPEED BUS	PERIODIC ON LINE DIAGNOSTICS	NON PERIODIC ON LINE DIAGNOSTICS TRAPS AND ABORTS	ROLL BACK	OFF LINE DIAGNOSTICS
HARDWARE ERROR DETECTION	• MAIN MEMORY: • DATA PARITY IP/BYTE* • CACHE MEMORY: • DATA PARITY IP/BYTE* • ADDRESS PARITY ZP/TAG • ADDRESSING ERRORS • ODD ADDRESS • NON-EXISTENT MEMORY	• NONE	• CPU ERRORS • ILLEGAL HALT • ODD ADDRESS • NON-EXISTENT MEMORY • UNIBUS TIMEOUT • STACK LIMIT • ILLEGAL OR RESERVED INSTRUCTIONS • POWER FAIL	• DEVICE CONTROLLERS CHECK DATA PARITY AND OTHER • DEVICE ERRORS • UNIBUS TIME OUT	• DEVICE CONTROLLERS CHECK DATA PARITY AND OTHER • DEVICE ERRORS	• NONE IN HARDWARE	TRAPS FOR LOC. • CPU ERRORS 4 • ILLEGAL & RESERVED INSTRUCTIONS 10 • IOT INPUT/OUTPUT 20 • POWER FAIL 24 • MEM. SYST. ERRORS 114 • FPP ERRORS 244 • MMU ERROR 250	• NONE IN CPU NO PROVISION TO SAVE STATUS FOR MORE THAN ONE INSTRUCTION (CURRENT ONE) • FPU HAS PROVISIONS FOR BACKUP AND RESTART FOR PARTIALLY COMPLETED INSTRUCTION (ABORT)	• ELECTRONIC CONSOLE FOR REMOTE DIAGNOSTICS THRU CENTRALIZED (DEC) FACILITY IN MARYLAND • MAINTENANCE REGISTERS
ERROR REPORTED IN	• MEMORY SYSTEM ERROR REGISTER • LOW ERROR ADDRESS REGISTER • HIGH ERROR ADDRESS REGISTER • (MAINTENANCE REG.)		• CPU ERROR REGISTER	• DEVICE STATUS REGISTER HAS ERROR BITS • PARITY ERROR LINES ON UNIBUS SET CPU ERROR LOG	• 3 CONTROL AND STATUS REGISTER HAVE ERROR BITS	• (ERROR LOGGING CAN BE PROVIDED BY THE O.S.)	• ERROR BITS SET IN THE CORRESPONDING ERROR OR STATUS REGISTERS	• ERROR AND STATUS REGISTERS	• ERROR AND STATUS REGISTERS
ACTION IN HARDWARE	• TRAP OR ABORT VIA LOC 114 OR 250 • HARDWARE PROVISION TO BYPASS 1/2 OR WHOLE OF CACHE (CONTROL REGISTER)		• HARD ERRORS TRAP VIA LOC. 4, 10, 24	• HARD ERROR TRAP VIA LOC. 4 • SOFT ERROR NONE	• HARD ERRORS • SOFT ERRORS NONE	• (ROM HARDWARE FOR THE BOOTSTRAP HAS BUILT IN DIAGNOSTIC TEST)	• CPU TRAPS TO PREDESIGNATED LOCATIONS (ADDRESSES)	• MMU BACKUP AND RESTART RECOVERY PROCEDURE	• NONE USUALLY TRAPS ARE DISABLED DURING OFF-LINE DIAGNOSTICS
ACTION IN SOFTWARE	• O.S. MUST PROVIDE TRAP HANDLERS FOR FAULT ISOLATION • MMU PROGRAMMABLE TO BYPASS BAD SECTIONS IN THE MAIN MEMORY		• O.S. MUST PROVIDE TRAP HANDLERS FOR FAULT ISOLATION	• O.S OR I/O HANDLERS MUST CHECK CONTROL AND STATUS REGISTERS TO CHECK SOFT ERRORS AND ISOLATE FAULTS • O.S. MUST PROVIDE TRAP HANDLERS TO ISOLATE FAULTS		• (POSSIBLE IN SOFTWARE RESPONSIBILITY OF THE O.S.)	• O.S. MUST PROVIDE TRAP HANDLER FOR FAULT ISOLATION		• SOFTWARE DIAGNOSTICS TEST PROGRAMS

*PARITY CHECKING

PARITY IS CHECKED FOR THE FOLLOWING BUS TRANSFERS

1. MAIN MEMORY -- CACHE MEMORY	ADDRESS + DATA
2. CACHE MEMORY -- CPU (MMU).	DATA ONLY
3. MAIN MEMORY -- HIGH SPEED I/O CONTROLLERS.	DATA ONLY
4. HIGH SPEED I/O CONTROLLERS -- MASS STORAGE DEVICES.	DATA ONLY

SYSTEM HANDLING OF HARD ERRORS (e.g. PARITY ERROR)

1. ABORT RIGHT THRU THE INSTRUCTION
2. TRAP AFTER THE INSTRUCTION IS COMPLETED.

3.5 AN/AYK-14(V)

The AN/AYK-14(V) is a standard airborne computer designed by the Control Data Corporation [21]. It is a subset of the recently developed CDC-480 computer family. The AN/AYK-14(V) computer system provides 16 module types which can be configured in various combinations in three different chassis types. This feature, like that of the MCF computer systems, makes it a variable configuration, general purpose minicomputer.

The AN/AYK-14(V) has several built-in-test features worth mentioning. Resident in the system are the BIT hardware, BIT firmware and In-Flight Performance Monitoring (IFPM) software which are used to detect and isolate a faulty computer chassis in the field. The faulty computer chassis sent to a shop level maintenance facility where a Loader/Verifier (L/V) is used to isolate the malfunctioning Shop Replaceable Assembly (SRA) through Fault Isolation Diagnostic (FID) software. The faulty SRA is forwarded to a repair facility at the depot level for isolation and repair of the faulty components through the use of Automatic Test Equipment (ATE). [21]

The fault detection and isolation features for the AN/AYK-14(V) are summarized in Table 3.4.

Table 3.4 AN/AYK-14(V) FAULT DETECTION AND ISOLATION FEATURES

	BIT Hardware		BIT Firmware	IFPM Software	FID Software
	Fixed	Programmable			
	CPU, Memory I/O Chassis Resident	CPU, I/O Chasses Resident	Micro Memory Resident	Main Memory Resident	Support Equipment, Mag. Tape Resident
	ON-LINE Continuous	OFF-LINE Used by I/O Test Software	OFF-LINE Initiated by •Power ON Sequence •Diagnostic Jump Instr.	OFF-LINE Used by the SDEX/14 O.S	OFF-LINE Loaded through L/V at Shop Level
Functions Checked	•Memory Parity •Memory Protect •Memory Channel Timeout •Overtemperature •Bus Timeout •I/O Channel Parity •I/O Channel Timeout •SIM Manchester Code Verification •BIT Timer •BIT Indicator	•I/O Wraparound •Computer Support Interface	Micro Coded Routines for: •Microsequence Test •Register Test •ALU Test •File & C-File Test •MCM Page File Test •Memory Interface Test •Firmware Event Test •PSM Interface Test	Assembly Language Routines for: •CPU/Memory Quick Look Test (CMQT) •I/O Tests (*) •Additional Memory Tests (*) •Additional CPU Tests (*)	Modular/Configurable Test Programs for: •Memory •Processor •I/O
Action	Generate Interrupts		•Run Micro Tests •Generate Interrupts •Supply Status/Isolation Code •Set BIT Indicator	•Process Interrupts •Run Macro Tests •Reset BIT Timer •Set BIT Indicator	•Run Modular Tests •Isolate Faults to SRA Level •Display Results on Cont. Panel or CRT
Confidence			High Level of Confidence	Fault Detection in 98% of All System Resources	Fault Isolation to 1 SRA 95% 2 SRAs 99%
	CHASSIS LEVEL FAULT DETECTION				SRA (Module) Level FAULT DETECTION & ISOLATION

4.0 MCF BUILT-IN-TEST DESCRIPTION AND ASSUMPTIONS

The primary objective of this section is to formulate a coherent structure for the built-in-tests to be specified for the MCF computer systems and define a set of guidelines from which specific recommendations for the built-in-test hardware and software can be developed. In the process of defining an overall built-in-test strategy, several assumptions have been made regarding the operation and maintenance of the MCF computer systems. These assumptions together with the concepts involved in designing built-in-test features are discussed in this section.

The major concepts presented in this section are given below. These concepts are not new and in the past some of these concepts have in fact been put into practice on military as well as commercial computer systems.

1. Distribution of responsibility for conducting built-in-test among three (3) hierarchical levels (module, chassis, and system levels) of the MCF computer systems.
2. Stand-alone, self-test capability at the chassis level for all chassis within the system.
3. User selectable/programmable built-in-test features to allow the BIT functions to be tailored to meet the requirements of a wide range of applications.
4. A building block or layered approach for conducting built-in-test. In this approach, the most basic hardware functions are tested first. Once the basic hardware blocks are checked out, they can be used in testing larger and more complex hardware functions. This approach reduces the total test equipment cost.
5. A provision for alternative, independent testing configurations to allow a degree of overlap or redundancy in the built-in-test. This implies having more than one way of testing a faulty element on the system. Although this increases the total test equipment required, it decreases the false alarms by cross checking (verifying the detected fault).

4.1 Three-Level Built-In-Test Hierarchy

It should be recalled from the description presented in Section 2.1 that the MCF computer systems are functionally partitioned into modules. These modules plug into a backplane within a chassis and communicate with each other via a common bus structure. A chassis when populated with an appropriate complement of modules forms a working subsystem. A set of chassis interconnected with cables forms a complete system.

Furthermore, recall that the chassis are of two basic types: 1) Main Computer Chassis, 2) Expansion Chassis. These two types of chassis differ in one important respect. The Main Computer Chassis contains the central intelligence of the system in the CPU3 module which is not available in the Expansion Chassis. In fact, in the single processor system in the MCF AN/UYK-41(V), the Main Computer Chassis No. 1 can by itself be operated as a complete system without any Expansion Chassis. However, no Expansion Chassis by itself can constitute a system. This distinction is important from the built-in-test viewpoint because certain degree decision making is required in performing all of the BIT functions mentioned in Section 2.3.3.

This type of a partitioned system structure lends itself to a similar partitioning in the implementation of built-in-tests. It is desirable to distribute the responsibilities of testing to the various hierarchical levels, namely, the module, chassis, and system levels, rather than concentrating them at any one level or delegating them to one particular module. The following built-in-test levels are to be identified:

1. Module Level BIT (MBIT)
2. Chassis Level BIT (CBIT)
    (a) Expansion Chassis BIT (ECBIT)
    (b) Main Computer Chassis BIT (MCBIT)
3. System (or Member) Level BIT (SBIT)

The Module Level BIT is the lowest level while the System Level BIT is the highest level. In order to distinguish between the BIT in the Main Computer and the Expansion Chassis, they have been assigned separate BIT levels.

4.2 Fault Coverage

One of the primary goals of the built-in-tests for the MCF computer system is to provide continuous system monitoring and indication of system malfunction. This implies that on-line fault detection and isolation together with local fault indication must be provided. It is conceived that this will be the primary responsibility of the Module Level BIT. The BIT at the module level has the advantage of being able to access the signals and test points internal to the module. Good observability is important in on-line testing. However, on-line testing has its disadvantage in that it is restricted to passive, non-interfering and non-disruptive techniques. This restriction places certain limitations on the fault coverage that can be obtained through on-line testing at module level.

In order to increase fault coverage, built-in-tests at chassis and system levels can be employed to test the hardware on the modules. Since the modules are defined as functional building blocks which are interconnected by common bus structure (data, address, and control paths), testing at a functional level is more appropriate. Functional level testing in this context implies generating an input test pattern to excite a certain function on the module and comparing the response to a predetermined value. This is an active form of testing. Active testing is usually done either off-line or during idle time because it is generally interfering and disruptive.

It should also be mentioned that apart from additional fault coverage, the chassis and system level tests may be used to provide fault verification and thereby reduce the false alarm rate. On-line tests at the module level typically will not discriminate between intermittent and stuck-at (solid) faults. Error logging and off-line tests are particularly useful for this reason which can be provided at the chassis and system levels.

4.3 Built-In-Test Objectives

In view of the above general discussion regarding the 3-level built-in-test hierarchy reasonable objectives should be set forth for the BIT at each level so that more detailed specifications can be developed. The following sections define these objectives.

4.3.1 Module Level Built-In-Tests

1. The Module Level BIT should provide adequate on-line, local fault detection for the hardware functions implemented on a given module.
2. It should provide a continuous indication of the module status (operate/failed) on the module.
3. It should communicate (report) all faults to the higher level BITs (chassis and system level).
4. It should assist the higher level BITs in performing idle time, periodic, or off-line tests to extend fault coverage.

4.3.2 Chassis Level Built-In-Tests

1. The Chassis Level BIT should provide additional fault coverage for modules within a chassis by using idle time, periodic, or OFF-line testing techniques.
2. It should provide an alternative, independent means for indicating faults detected in any module within the chassis. This is in addition to and separate from the fault indicators on the modules.
3. It should assist the higher level BIT (system level) in idle time, periodic or off-line testing of modules within a chassis.
4. It should assist the higher level BIT in communicating, logging, and characterizing of all faults detected within a chassis in on-line mode.
5. It should provide an alternative, stand-alone means for testing the modules within a chassis in an off-line mode.

4.3.3 System Level Built-In-Tests

1. The System Level BIT should provide additional fault coverage for all modules within the system by using idle time, periodic, or off-line testing techniques.
2. It should provide means for logging, characterizing of all faults detected within the system in on-line mode.

3. It should report the faults to the operator.
4. It should provide an interface with the operator for trouble-shooting and general maintenance of the system.

4.4 Built-In-Test Resource Characterization

In order to realize the above mentioned objectives of the built-in-tests, certain hardware and software resources would be required at each of the three levels.

At the module level, the BIT functions performed are mainly fault detection, indication, and communication. Fault detection and isolation are synonymous at this level because the faults have to be localized only to a module. It is possible to implement these BIT functions using non-intelligent, fixed and programmable hardware logic cirucits which can reside on the module. The programmable hardware will be required to externally enable certain BIT features to facilitate the testing of the hardware on the module from the Chassis or System Level BITs.

The Chassis Level BIT is responsible for testing all of the modules (including itself) within a chassis. It must, therefore, be capable of providing almost all of the BIT functions with the exception of error handling which can only be done at the system level. It must also perform active tests on the modules. For these reasons, it is envisioned that at the Chassis Level the built-in-tests can best be implemented using intelligent hardware with certain decision making capability such as a microprocessor. This intelligent hardware may be supported by software in local storage. Typical software would consist of test patterns and simple diagnostic routines. Furthermore, the Chassis Level BIT hardware and software may be placed in a separate module within the chassis. A single Chassis Level BIT module may be designed which can be programmed to meet the built-in-test requirements of the various types of chassis. In addition, a simple maintenance panel accessible to the operator may be added to each chassis on which the fault signature may be displayed. This maintenance panel should also have a few switches with which the operator can initiate the chassis level diagnostics. Such an arrangement will provide a stand-alone self-test capability at the chassis level.

The System Level BIT will reside in the Main Computer Chassis where the microcode and intelligence of the CPU module can be used. It is

assumed that most of the built-in-tests at the system level will be software or firmware based. The diagnostic software may be placed in non-volatile main memory or may be resident on an external mass storage media. It is also assumed a sophisticated system console panel will be available which can be used by the operator to control the CPU during both normal and maintenance operations. During normal operations, the operator can input regular commands to the operating system. During maintenance testing, the operator should be able to directly access those CPU functions via the console panel that make diagnosis possible. Furthermore, it is envisioned that the console panel function may be extended to not only provide on-site (local) diagnostic facility, but optionally also provide a capability to conduct diagnosis from a remote site.

The Table 4.1 summarizes the characteristics of the BIT hardware and software resources required to implement the built-in-tests at the three hierarchical levels.

4.5 Built-In-Test Equipment Configuration and Interface Definition

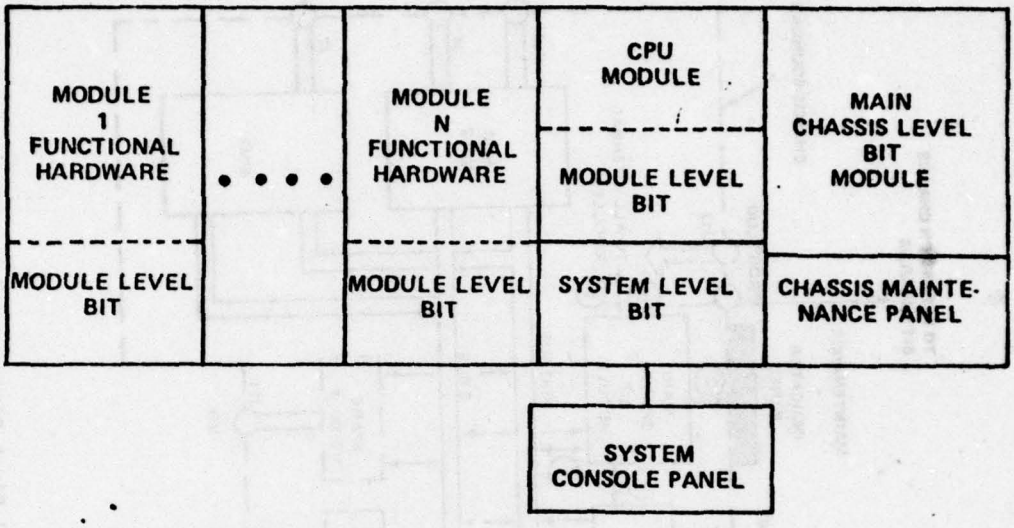
The diagrams in Figure 4.1 help visualize the physical placement of the above discussed built-in-test equipment (BITE).

More detailed block diagrams including the additional built-in-test equipment are shown for each type of MCF chassis in Figures 4.2, 4.3, 4.4, and 4.5. From these block diagrams, general interface definitions can be involved for communication among the 3-levels of built-in-tests and other constituent modules of the MCF computer systems. These interfaces are identified in Figures 4.2 through 4.5 by letters A, B, C, D, and E. The definitions and functions of these interfaces are given below.

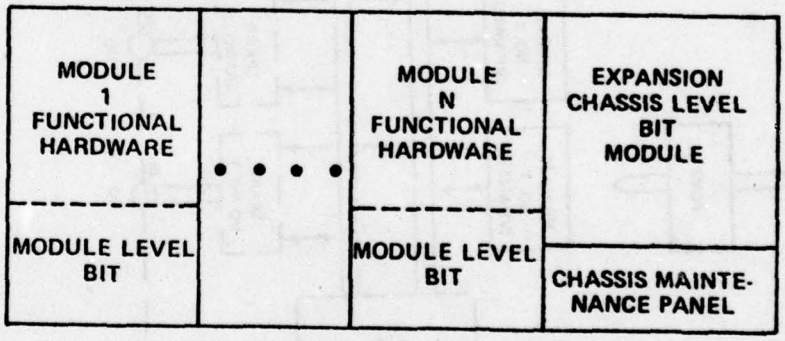
A. Interface between Chassis Level BIT Module and all other MCF modules. This interface uses the existing MCF bus structure and will be used for two purposes. 1) To allow the Chassis Level BIT Module to conduct idle time or off-line tests on all other MCF modules within the chassis. 2) To directly report any detected faults to the CPU module.

TABLE 4.1 SUMMARY OF THE MCF BIT RESOURCES

Hierarchical BIT Level	BIT Resource Characteristics
Module	(a) Non-intelligent fixed and programmable hardware resident on the module
Chassis	(a) Intelligent hardware and diagnostic software (or firmware) resident on a separate module within the chassis (b) A maintenance panel on the chassis accessible to the operator.
System	(a) Intelligent hardware and diagnostic firmware resident on the CPU module (b) Diagnostic software resident on non-volatile main memory and/or on external mass storage device (c) A system console panel with local and remote diagnosis capability



(a) Main Computer Chassis



(b) Expansion Chassis

Figure 4.1 MCF Built-In-Test Equipment Configuration

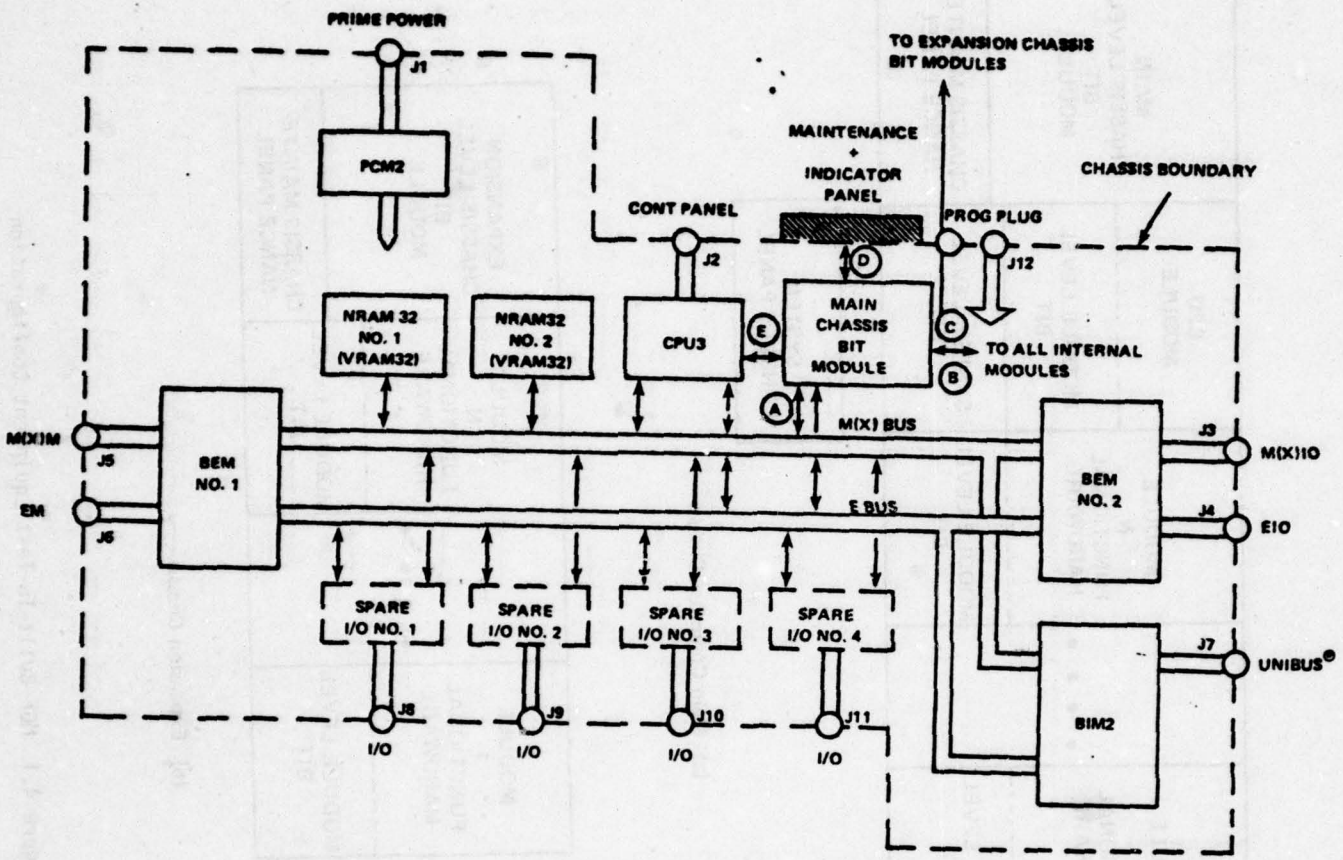


Figure 4.2 AN/GYQ-21 (V) Main Computer Chassis No. 1 Block Diagram with Additional Built-In-Test Equipment [9]

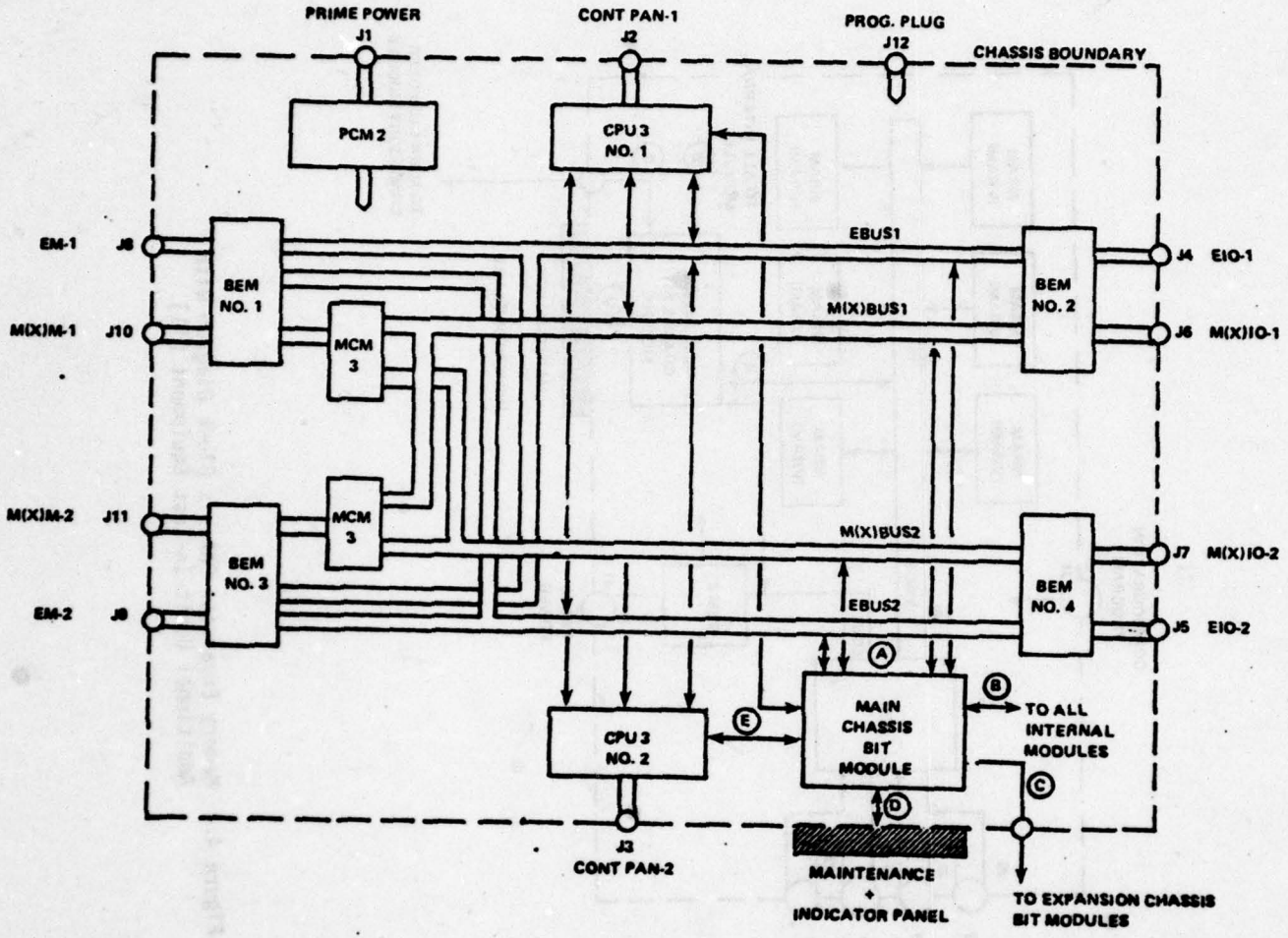


Figure 4.3 AN/GYQ-21 (V) Main Computer Chassis #2 Block Diagram with Additional Built-In-Test Equipment [10]

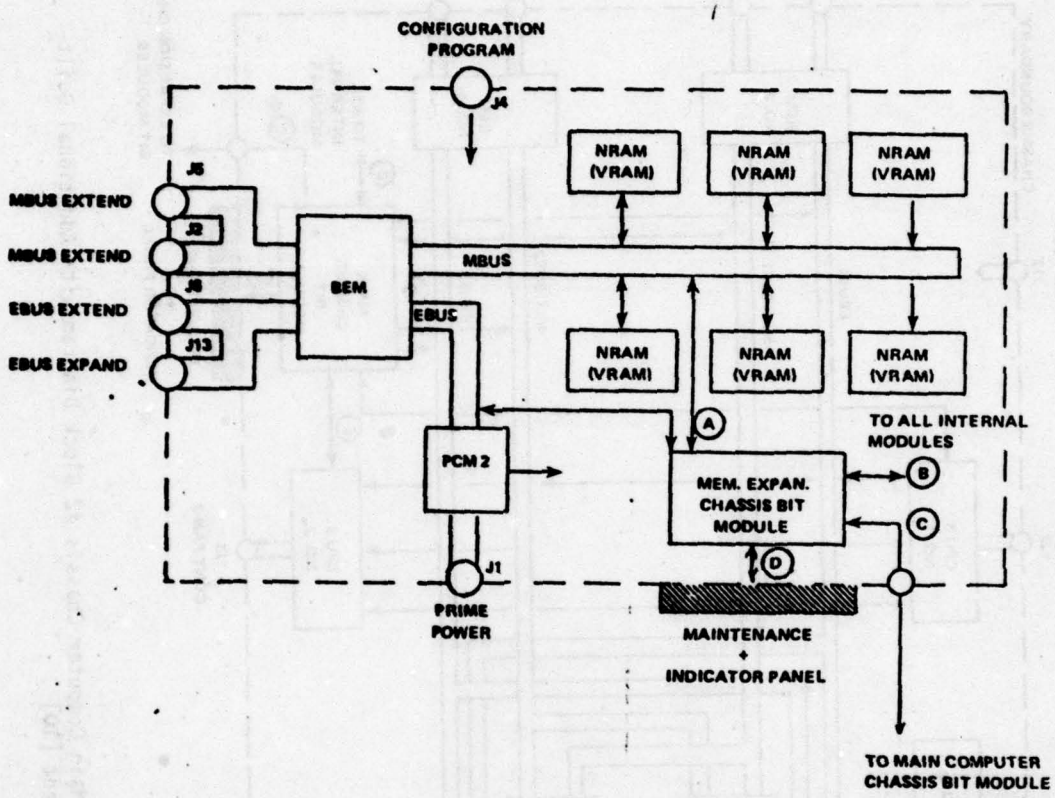


Figure 4.4 Memory Expansion Chassis Block Diagram with Additional Built-In-Test Equipment [11]

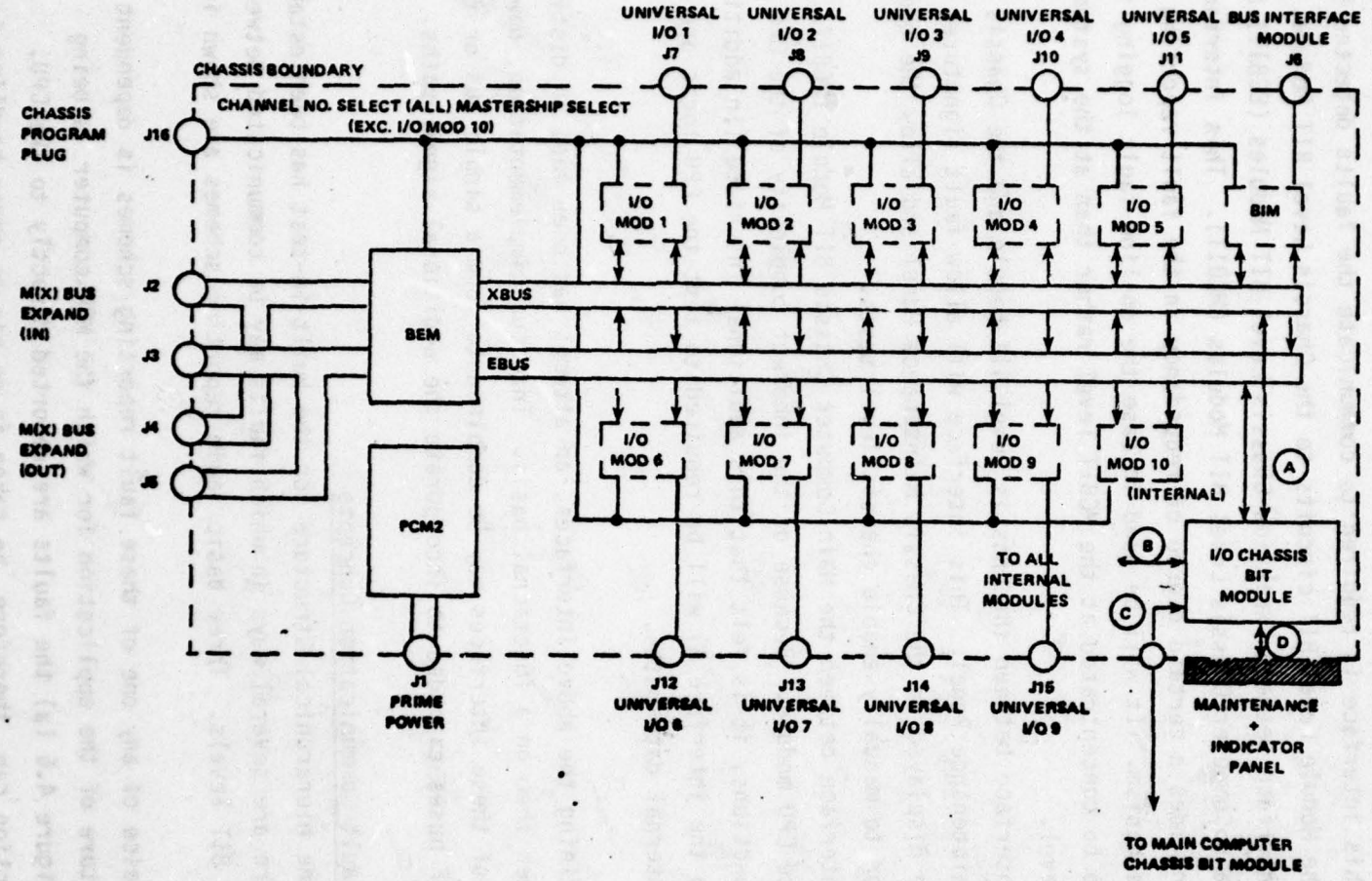


Figure 4.5 I/O Expansion Chassis Block Diagram with Additional Built-In-Test Equipment [12]

B. Interface between Module Level BIT and Chassis Level BIT Module. This interface is required to communicate the faults detected by the Module Level BIT circuits to the Chassis Level BIT Module.

C. Interface between Expansion Chassis Level BIT Modules (ECBIT) and Main Computer Chassis Level BIT Modules (MCBIT). This interface provides a certain degree of redundancy in the fault reporting mechanism. It will be used in case the on-line fault logging is to be concentrated at the MCBIT level rather than at the system level.

D. Interface between the Chassis Level BIT Module and the Chassis Maintenance Panel. This interface will allow fault signatures to be displayed on the Chassis Maintenance Panel and allow the operator to manually enable chassis level tests.

E. Interface between the Main Computer Chassis BIT Module (MCBIT) and the CPU module. Because of the inherent complexity of the CPU functions, it is felt that this additional interface (in addition to the interface A) will be required to test the CPU logic and internal data paths.

In defining the above interfaces, an attempt has been made to distinguish between them on a functional basis. In actual implementation, however, some of these interfaces may be combined to form a single bus or the existing MCF buses expanded to incorporate the additional signal paths.

4.6 Fault Communication Concepts

Once the hierarchical structure for the built-in-test has been established, there are several ways in which faults may be communicated between the various BIT levels. Three basic fault reporting schemes are shown in Figure 4.6.

The choice of any one of these fault reporting schemes is dependent upon the nature of the application for which the MCF computer is being used. In Figure 4.6 (a) the faults are reported directly to the CPU. Immediate action can, therefore, be taken in so far as error handling is concerned. This scheme is useful in applications where a system malfunction can produce harmful results such as in automatic feedback control systems. In contrast, in the scheme shown in Figure 4.6 (c), all faults

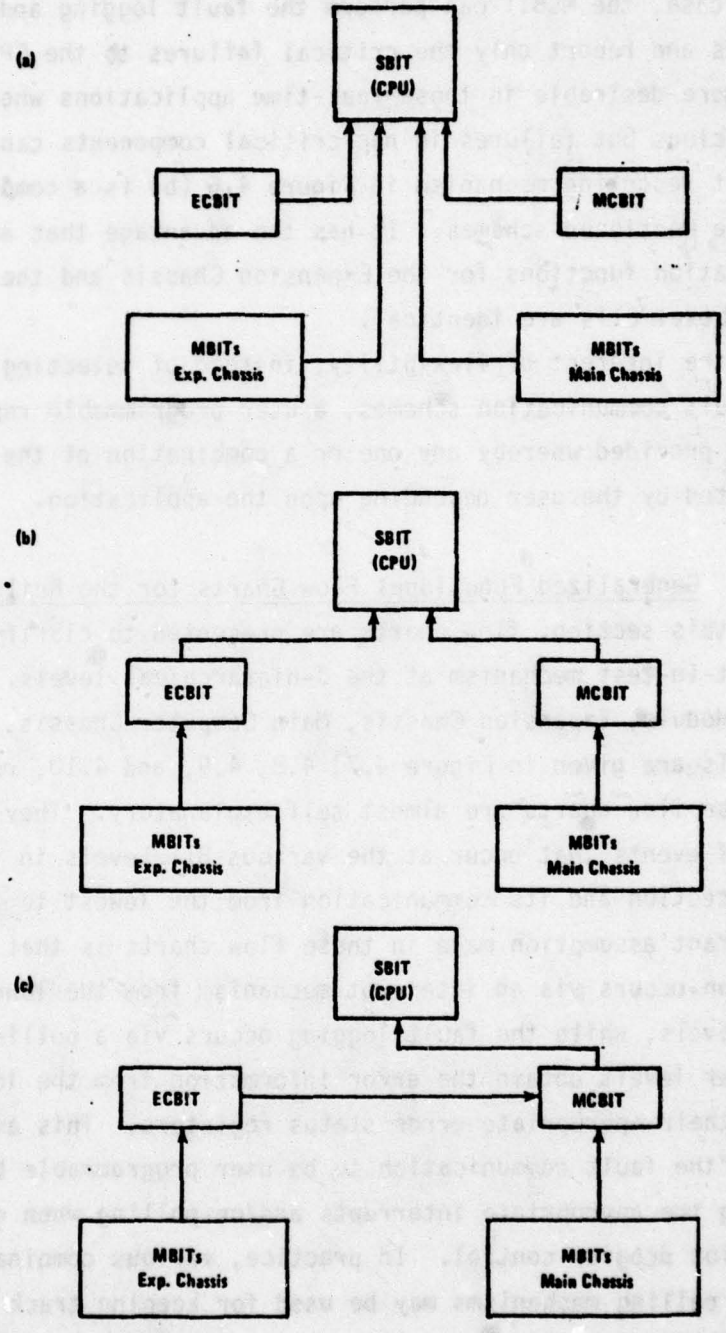


Figure 4.6 Alternative Fault Communication Schemes

are reported to the CPU via the Main Computer Chassis BIT Module (MCBIT). In this case, the MCBIT can perform the fault logging and characterization functions and report only the critical failures to the CPU. Such schemes may be more desirable in those real-time applications where the CPU time is more precious but failures in non-critical components can be tolerated. The fault reporting mechanism in Figure 4.6 (b) is a compromise between the two above mentioned schemes. It has the advantage that at least the fault communication functions for the Expansion Chassis and the Main Computer Chassis Level BITs are identical.

In the interest of flexibility, instead of selecting any one of the above fault communication schemes, a user programmable reporting hardware could be provided whereby any one or a combination of the above schemes may be selected by the user depending upon the application.

4.7 Generalized Functional Flow Charts for the Built-In-Tests

In this section, flow charts are presented to clarify the operation of the built-in-test mechanism at the 3-hierarchical levels. The flow charts for the Module, Expansion Chassis, Main Computer Chassis, and the System Level BITs are given in Figure 4.7, 4.8, 4.9, and 4.10, respectively.

These flow charts are almost self explanatory. They describe the sequence of events that occur at the various BIT levels in the process of fault detection and its communication from the lowest to the highest level. An important assumption made in these flow charts is that the fault communication occurs via an interrupt mechanism from the lower levels to the higher levels, while the fault logging occurs via a polling mechanism where the higher levels obtain the error information from the lower levels by reading their appropriate error status registers. This assumption was made to allow the fault communication to be user programmable by enabling or disabling the appropriate interrupts and/or polling when desired under application program control. In practice, various combinations of interrupt and polling mechanisms may be used for keeping track of the health status of the system.

These flow charts have been generalized to cover on-line, idle time, and off-line fault monitoring techniques. They also show the stand-alone, self-test mode at the chassis level.

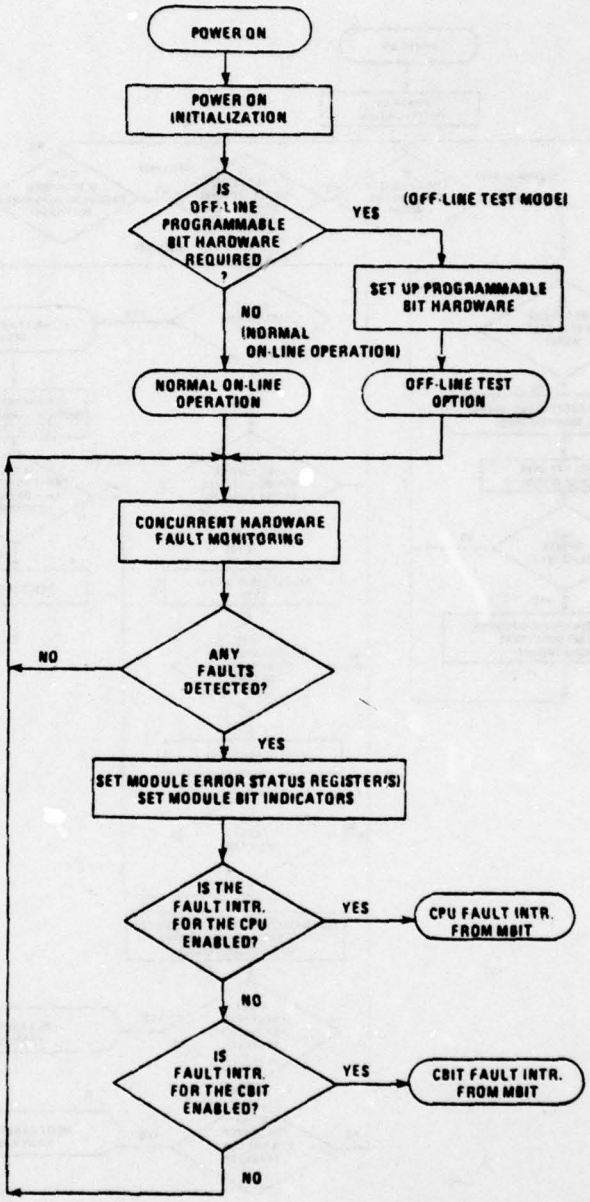


Figure 4.7 Module Level BIT (MBIT) Functional Flow Chart for On-Line and Off-Line Cases

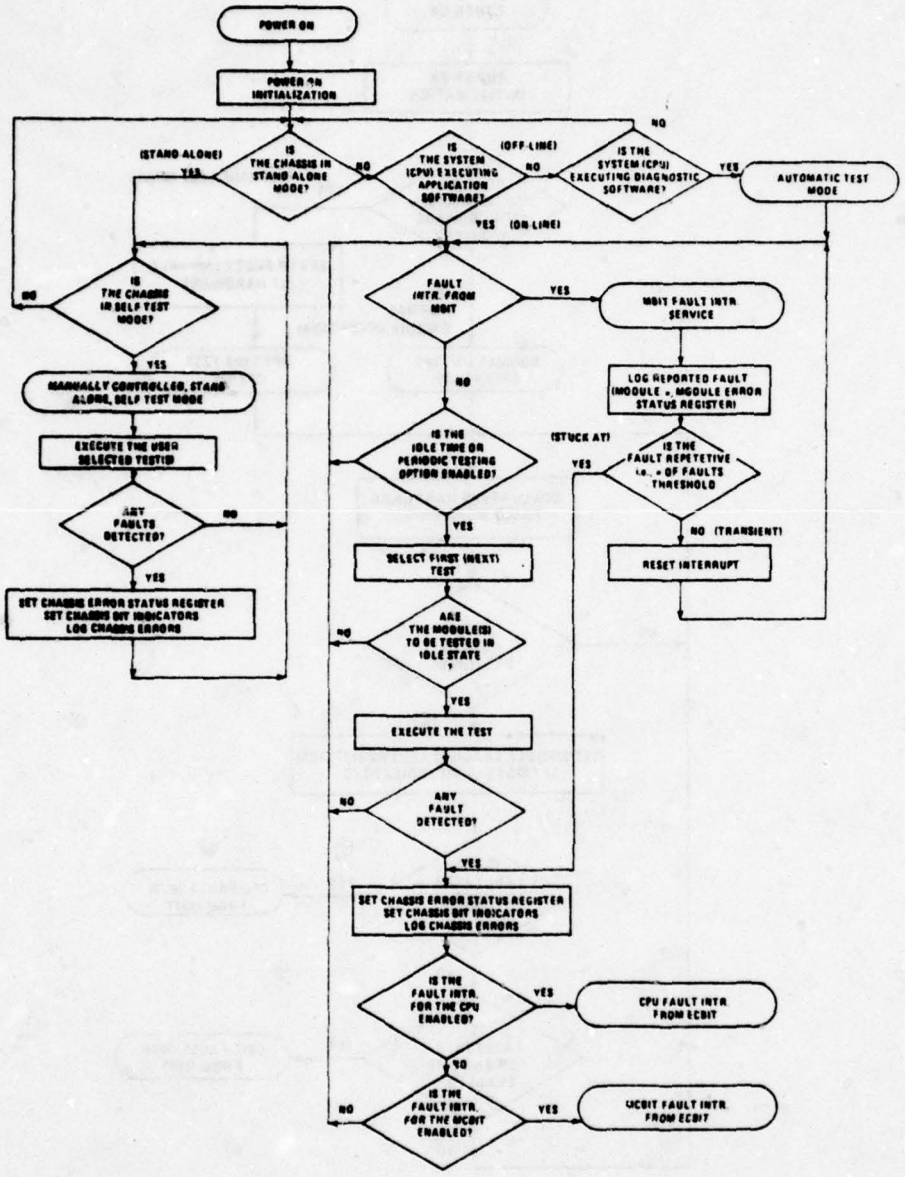


Figure 4.8 Expansion Chassis Level BIT (ECBIT) Functional Flow Chart For On-Line, Idle Time, and Off-Line Cases

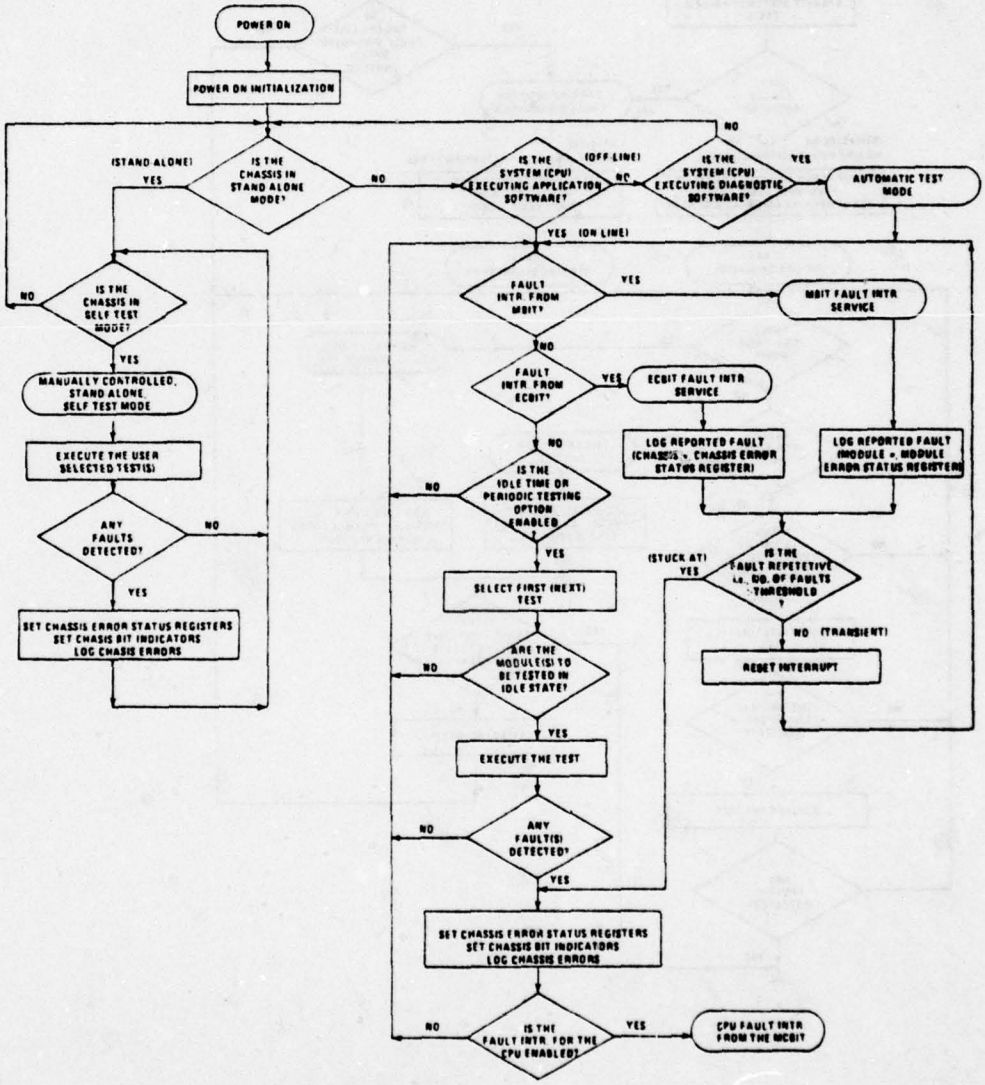


Figure 4.9 Main Chassis Level BIT (MCBIT) Functional Flow Chart For On-Line, Idle Time, and Off-Line Cases

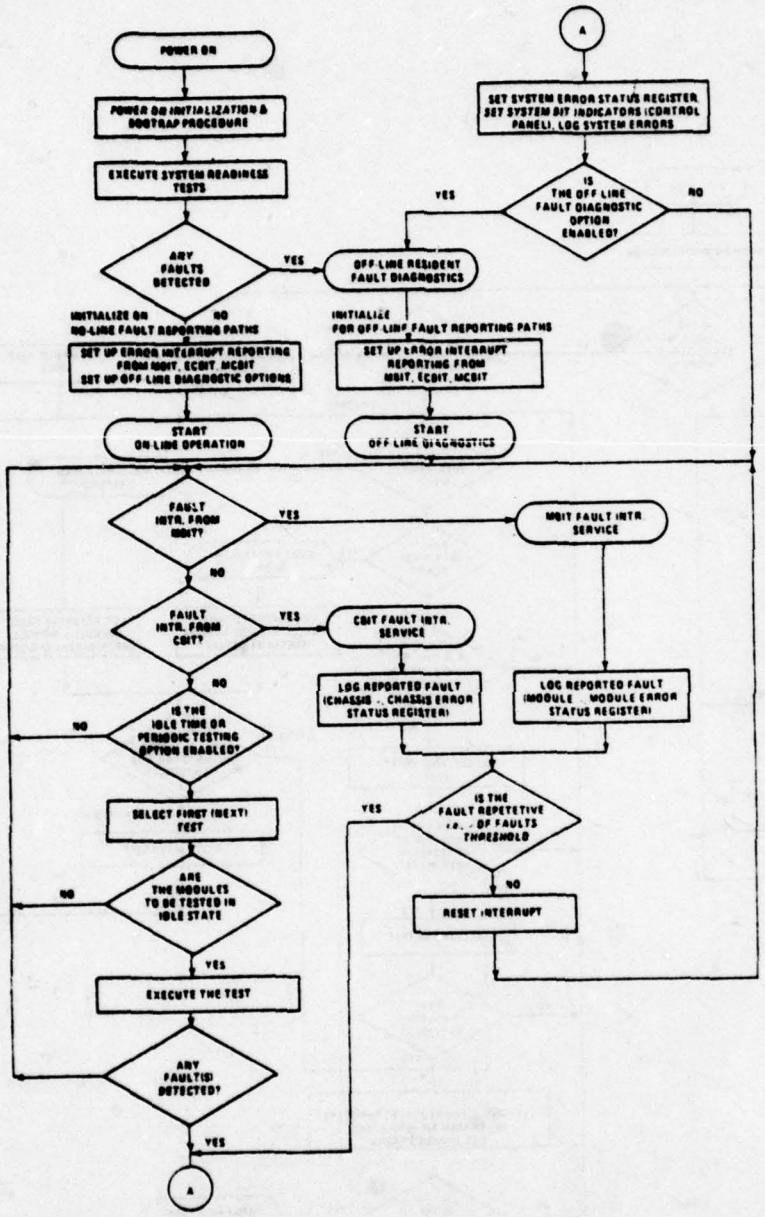


Figure 4.10 System Level BIT (SBIT) Functional Flow Chart For On-Line, Idle Time, and Off-Line Cases

4.8 Basic System Test Configurations

One of the motivations in recommending a Chassis Level BIT is to provide a stand-alone, self-test capability for each chassis within the system. An advantage of this is that if hardware in a certain chassis is suspected to be malfunctioning that chassis may be disconnected from the system for test purposes. While the chassis is being tested in self-test mode to localize the fault, the system can at least be operated in a reduced configuration. This way the entire system resources need not be tied up during maintenance. Figure 4.11 (a) depicts the test configuration for the stand-alone chassis level tests.

In case of a complete system failure, the testing should begin in a building-block fashion. First, the System Console Panel should be used to check out the hard core logic (microsequencer and micromemory operations). Following that microdiagnostics can be invoked to test the basic CPU functions. If necessary, microdiagnostics may be loaded into micromemory from the external mass storage device via the system console panel. This basic CPU test configuration is shown in Figure 4.11 (b). Microdiagnostics may also be used to check the cache memory (if present), main memory and its associated data paths.

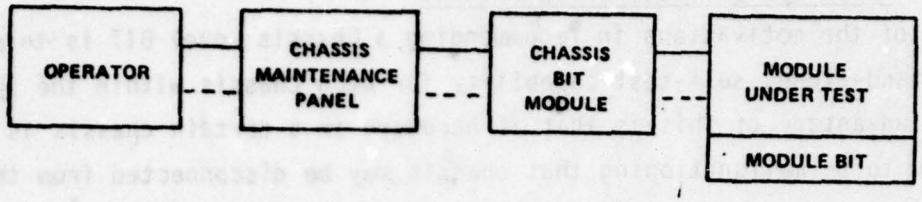
The remaining portions of the system can then be tested under CPU control using macrodiagnostic software as shown in Figure 4.11 (c). The macrodiagnostics should include functional and reliability tests for all modules and system peripheral devices (disks, magtapes, line printers, etc.).

4.9 Built-In-Test Functional Specifications

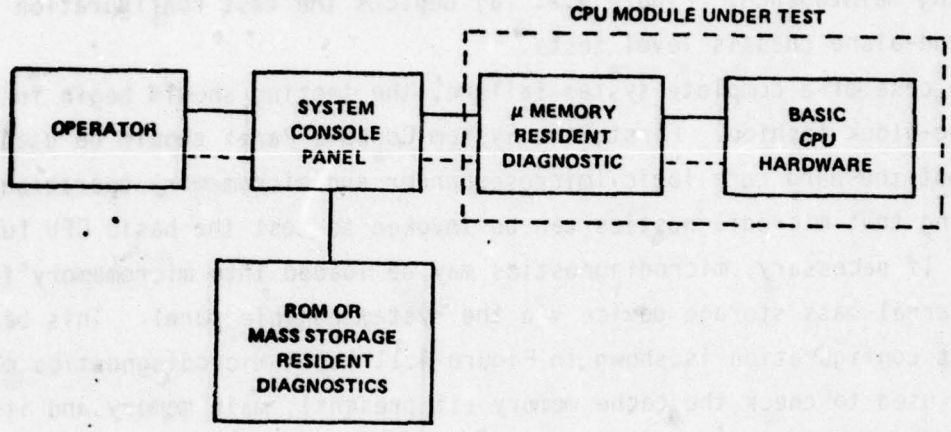
In view of all the discussions regarding the 3-level approach for built-in-tests presented so far, the following more detailed functional specifications can now be formulated.

4.9.1 Module Level Built-In-Tests

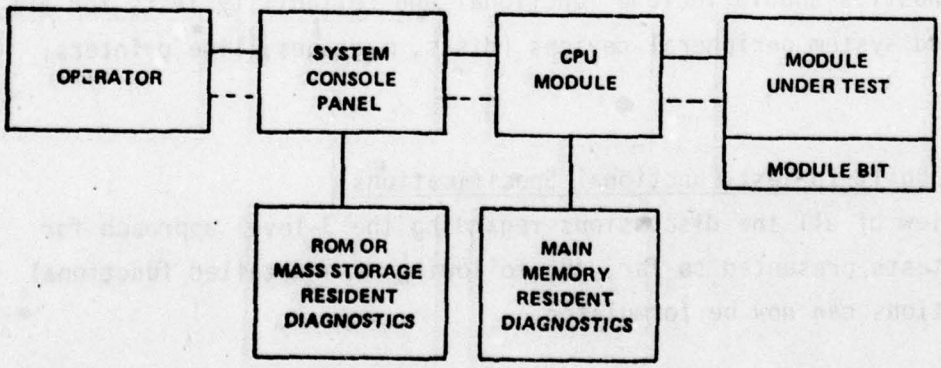
1. Continuously detect, using additional test hardware logic, faults within the module when the module is on-line. This should be done by partitioning the module into simpler logical subfunctions and providing a passive test logic for each subfunction.



(a) Stand-Alone Chassis Level Test Mode



(b) Basic CPU Test Under System Console Panel



(c) Full System Test Under CPU Control

Figure 4.11 Basic MCF Test Configurations

2. Log the type of error detected in error status register(s) on the module. The error status register(s) should be accessible to the higher level BITs. Furthermore, error status register once set should only be cleared by either the system reset signal or by command from the higher level BITs.
3. Be capable of reporting the fault condition via user programmable hardware interrupt option to the
    (a) System Level BIT in the CPU module
    (b) Chassis Level BIT Module.
4. Report all detected faults to the operator via non-volatile indicators placed on the module.
5. Be capable of aiding the Chassis and System Level BITs via programmable hardware logic to conduct fault detection and isolation tests when the module is in idle state or off-line. The faults being detected may lie
    (a) within the module
    (b) in external data paths (input/output lines) connected to the module
    (c) in other modules.

    The additional hardware logic used for this purpose should be programmed through and maintenance register(s) or maintenance bits in error status register(s) specially provided for this purpose.
6. Measure and record separately on each module in non-volatile form the accumulated elapsed time for which the power has been applied to that module.

4.9.2 Chassis Level Built-In-Tests

1. Continuously monitor all faults being reported by lower level BITs.
    (a) For the Expansion Chassis Level BIT the lower levels are the BITs on the modules within the chassis.
    (b) For the Main Computer Chassis Level BIT the lower levels are the BITs on the modules within the Main Computer Chassis and the Expansion Chassis Level BIT Modules.

2. Log the type of fault reported and the identity of the module reporting it in a non-volatile store on the Chassis Level BIT Module. This may be done by reading the error status register(s) of the faulty module.
3. Be capable of characterizing the reported faults into at least repetitive or non-repetitive classes (stuck-at or transient faults) by counting the number of occurrences. This can be done by analyzing the fault log on the Chassis Level BIT Module.
4. Be capable of reporting the fault conditions via user programmable hardware interrupt option to the higher level BITs.
   (a) For the Expansion Chassis Level BIT the higher levels are the Main Computer Chassis Level BIT Module and the System Level BIT in the CPU module.
   (b) For the Main Computer Chassis Level BIT the higher level is the System Level BIT in the CPU module.
5. Report all faults or fault signature to the operator via indicators, or numeric displays or small alpha-numeric printer on the Chassis Maintenance Panel.
6. Be capable of executing a selected test or tests (resident in non-volatile memory on the Chassis Level BIT Module) to detect and isolate hardware faults in all modules within the chassis if commanded by the operator via the Chassis Maintenance Panel when the chassis is in stand-alone mode.
7. Be capable of executing idle time test or tests (resident in non-volatile memory on the Chassis Level BIT Module) to detect and isolate hardware faults on all modules within the chassis when command by the System Level BIT via the CPU.
8. Measure and record separately on each chassis in non-volatile form the accumulated elapsed time for which power has been applied to that chassis.

4.9.3 System Level Built-In-Tests

1. Continuously monitor all faults being reported by lower level BITs, i.e., all Module Level BITs within the system, and the Expansion Chassis and Main Computer Chassis Level BIT Modules.

2. Log the type of fault reported and the identity of the source reporting it in a non-volatile store in the main memory or a file on a mass storage device.
3. Be capable of characterizing the reported faults into at least repetitive or non-repetitive classes (stuck-at or transient) by counting the number of occurrences. This can be done by analyzing the fault log mentioned in Item 2.
4. Be capable of reporting fault conditions (via user programmable software option) to the operator in one or more of the following ways.
   (a) Indicators on the System Console Panel
   (b) Indicators on the Main Computer Chassis Maintenance Panel
   (c) Printed message on any system output device.
5. Be capable of executing a selected test or tests, resident in non-volatile system memory, to detect and isolate faults in all modules within the system when commanded by the operator via the System Console Panel.
6. Be capable of executing test or tests, resident in non-volatile system memory, to detect and isolate faults in all modules within the system when initiated by the user via software instructions.
7. Be capable of executing a selected test or tests (resident in non-volatile micro-memory of the CPU module) to detect and isolate faults in the CPU module when initiated in one of the following ways:
   (a) by the user via a software instruction
   (b) by the operator via the System Console Panel
   (c) by the Main Computer Chassis Level BIT module.

4.10 Summary of the Built-In-Test Functions

The built-in-test features discussed in this section for the MCF computer systems are summarized in Table 4.2. The seven major functions discussed in this section are listed in the left-most column of Table 4.2. The responsibilities of the Module, Chassis, and System Level BITs during on-line, idle time, and off-line testing are shown in adjacent columns.

TABLE 4.2. SUMMARY OF THE BUILT-IN-TEST AND FUNCTIONS FOR THE MCF MODULE, CHASSIS AND SYSTEM LEVEL BITS.

Functions	Module Level BIT			Chassis Level BIT			System Level BIT		
	ON Line	Idle Time	OFF Line	ON Line	Idle Time	OFF Line	ON Line	Idle Time	OFF Line
1. Detection	✓	X	✓	X	✓	✓	X	✓	✓
2. Isolation	✓	X	✓	X	✓	✓	X	✓	✓
3. Indication to Operator	✓	X	✓	✓	✓	✓	✓	✓	✓
4. Reporting to Higher Level BIT	✓	X	✓	✓	✓	✓	✓	✓	✓
5. Logging in Local Storage	✓	X	✓	✓	✓	✓	✓	✓	✓
6. Characterization Stuck-at/Transient	X	X	X	✓	✓	✓	✓	✓	✓
7. Error Handling	X	X	X	X	X	X	✓	✓	✓
Test Domain	All Hardware Functions Within A Module			All Modules Within A Chassis			All Modules Within A System		

5.0 BUILT-IN-TEST RESOURCE ALLOCATION BASED ON FAILURE RATE ANALYSES

It is important in the design of maintainable digital computer systems to know which subsystems are most likely to fail. To do this precisely requires detailed knowledge of the particular circuits to be used in the synthesis of various parts of the computer system. In cases where the exact hardware embodiment is not known, it is reasonable to extrapolate from failure rates predicted for closely related machines.

A first cousin of the Military Computer Family member, AN/UYK-41, is the Digital Equipment Corporation's PDP-11/70. The DEC PDP-11/70 is therefore used in the following analysis to make inferences about the functional areas within the AN/UYK-41 which are most likely to fail. In addition, this same reasoning can be used to predict the failure rate increase for representative BIT approaches. The following sections summarize the PDP-11/70 analysis.

5.1 Objectives of the Failure Rate Analyses

The two major objectives of the failure rate analysis were: 1) to identify specific areas of the computer system that are most prone to failure, and 2) to predict the impact of BIT on the total system's failure rate. The basic premise here is: once the specific areas (modules, subsystems) that have high failure rates are found, these areas can be given the emphasis in the allocation of BIT resources. In this manner, the smallest amount of BIT hardware will detect the greatest number of errors. Another result of this analysis is the identificaiton of certain modules that have a failure rate so high that the use of error correcting hardware may be included in the design for meeting the MTBF specification. The failure rate model used in this analysis is that of MIL-HDBK-217B. For a more complete description of the model or definitions of various parameters, refer to that handbook.

5.2 Results of DEC PDP-11/70 Failure Rate Analysis

Using a computer program developed at Carnegie-Mellon University (CMU) called Autofail, it is possible to compute the failure rate of each board in the PDP-11/70 mainframe. While the 11/70 is not a military

computer, it represents a commercial machine with similar performance specifications to the MCF machines. The CMU program utilizes the electronic components failure rate model in MIL-HDBK-217B. The computer program does not use the exact modifications that are included in the two revisions to 217B, rather it uses a slightly different modification that approximates it.

Tables 5.1 and 5.2 represent a summary of this analysis. The computer was divided into the four units: CPU, floating point processor, cache, and main memory. For each of these units, the number of boards, the failure rate, and the percentage of total failure rate is given. Table 5.1 gives this information for the computer modules at an ambient temperature of 25°C, whereas Table 5.2 gives this same information at 85°C. The latter temperature was chosen because it is the specification in the ITEC documents [14].

One can easily see that memory failures dominate (92%) all others at high temperatures and are still a large percentage (50%) even at room temperature. The great influence that temperature has on the relative failure rate is discussed in Section 5.3. The next largest unit that is prone to failure is the CPU. Its failure rate is about twice that of the other two units. The numbers in Tables 5.1 and 5.2 represent a computer with no built-in-test so the numbers are not influenced by additional BIT hardware. In order to provide the best fault coverage at the lowest cost, the two areas that deserve the most consideration are the main memory and the CPU. By providing a high level of confidence in the proper operation of these two vital areas (through the use of BIT hardware) a high level of confidence in the operation of the computer is achieved. In fact, if these two vital areas are functioning properly, they can be used to check the other two areas; the cache memory, and the floating point processor. For more detailed information on the boards and components in each of the segments of the computer, a complete listing is included in Appendix B.

5.3 Comparison of Failure Rates Between MOS and Bipolar Technologies

There is a large difference between semiconductor technologies with respect to the effect of temperature on the failure rate. This fact was

TABLE 5.1. FAILURE RATE OF PDP-11/70 at 25°C

Subsystem	Number of P.C. Boards	Failure Rate C/10^6 Hr.	Percentage of Total Failure Rate (%)
Central Processing Unit	9	152	25
Floating Point Processor	4	89	15
Cache Memory (1K by 16 bits)	4	66	11
Main Memory (64K by 16 bits)	4	296	49
Total	25	603	100

TABLE 5.2. FAILURE RATE OF PDP-11/70 at 85°C

Subsystem	Number of P.C. Boards	Failure Rate (/10^6 Hr.)	Percentage of Total Failure Rate (%)
Central Processing Unit	9	383	4
Floating Point Processor	4	263	2
Cache Memory (1K by 16 bits)	4	199	2
Main Memory (64K by 16 bits)	4	9910	92
Total	25	10755	100

shown in Section 5.2 where the memory portion of the computer accounted for nearly all the failure rate (92%) at high temperature (85°C), but not at lower temperature. The memory boards are made up of mostly MOS chips that have a large failure rate acceleration with temperature. In contrast, the CPU boards are composed mainly of SSI & MSI chips whose failure rate has a much lower temperature dependence.

From an examination of the reliability model of MIL-HDBK-217B, one notices that bipolar technology has one temperature acceleration function whereas MOS technology has a different (larger) one. Figure 5.1 shows these two temperature factors (π_T). It is clear from this figure that the reliability of MOS devices degrades substantially at elevated temperatures. This means that a significant failure rate reduction can be achieved simply by keeping the ambient temperature a few degrees cooler!

To illustrate the impact that technology and temperature makes on the reliability Figure 5.2 graphically represents the failure rate as a function of temperature for the PDP-11/70. The components of this computer are classified into one of two groups: 1) ROM and RAM, or 2) SSI and MSI. The ROM and RAM group is predominately MOS and is made up of 472 chips. The SSI/MSI groups is predominately bipolar and is composed of 1870 chips. The larger number of MSI/SSI chips have about the same failure rate at room temperature as the memory because they are largely simple functions that each have a low failure rate. The memory chips are much more complex (i.e. more gates/chip) and, therefore, have a higher failure rate per chip. However, an interesting situation arises when the temperatures of each are increased. The memory's failure rate increases dramatically while the failure rate of the SSI/MSI group increases only slightly. This illustrates the fact that at elevated temperatures the memory portion of a computer will account for nearly all the hardware failures.

5.4 Failure Distributions of Other Computers

To get a somewhat broader view of reliabilities from a variety of computers, the following information is given. This reliability data was obtained from Carnegie-Mellon University from their continuing research on computer reliability. The data was derived from the model in MIL-HDBK-217

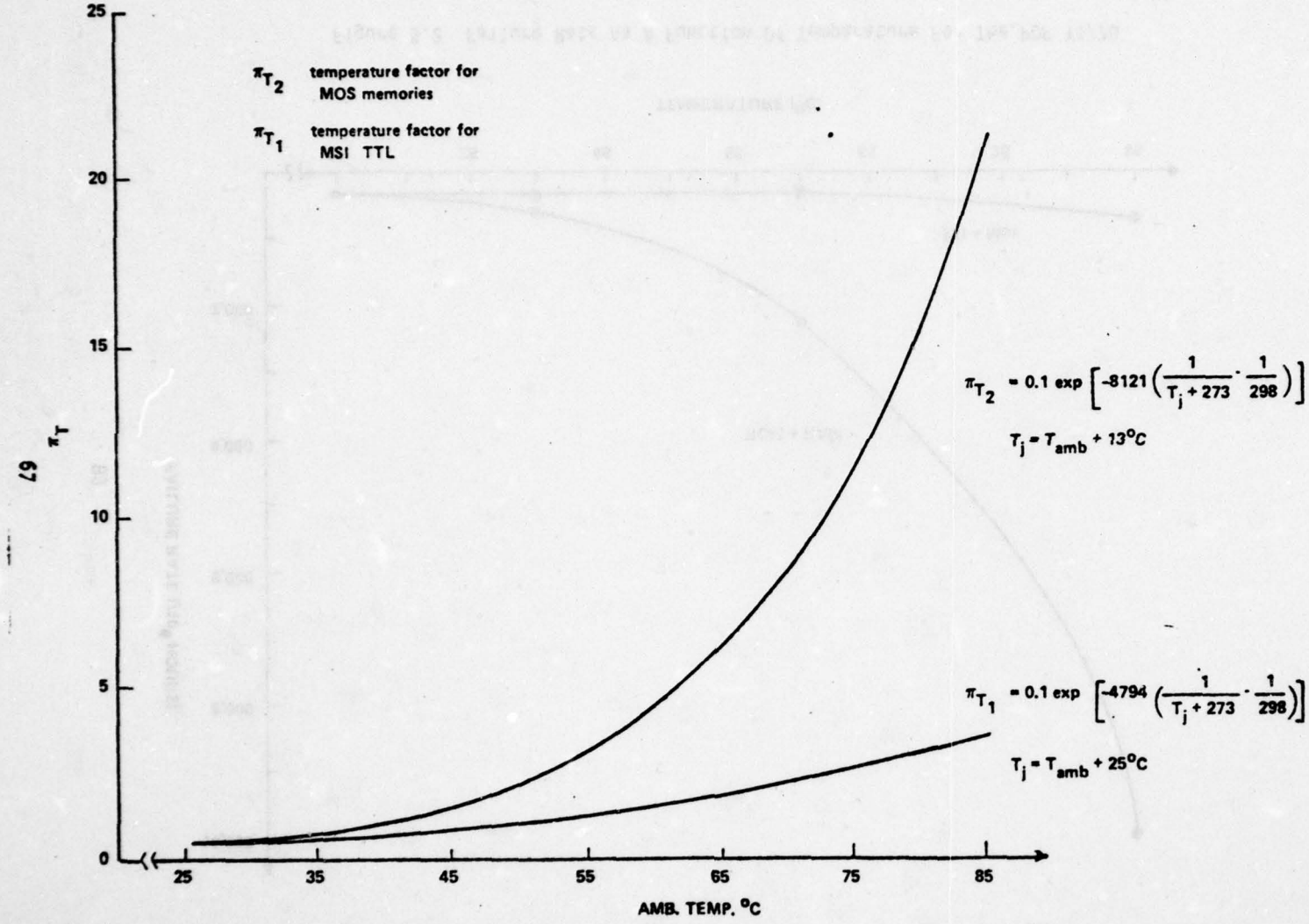


Figure 5.1 Curves of Temperature Factors

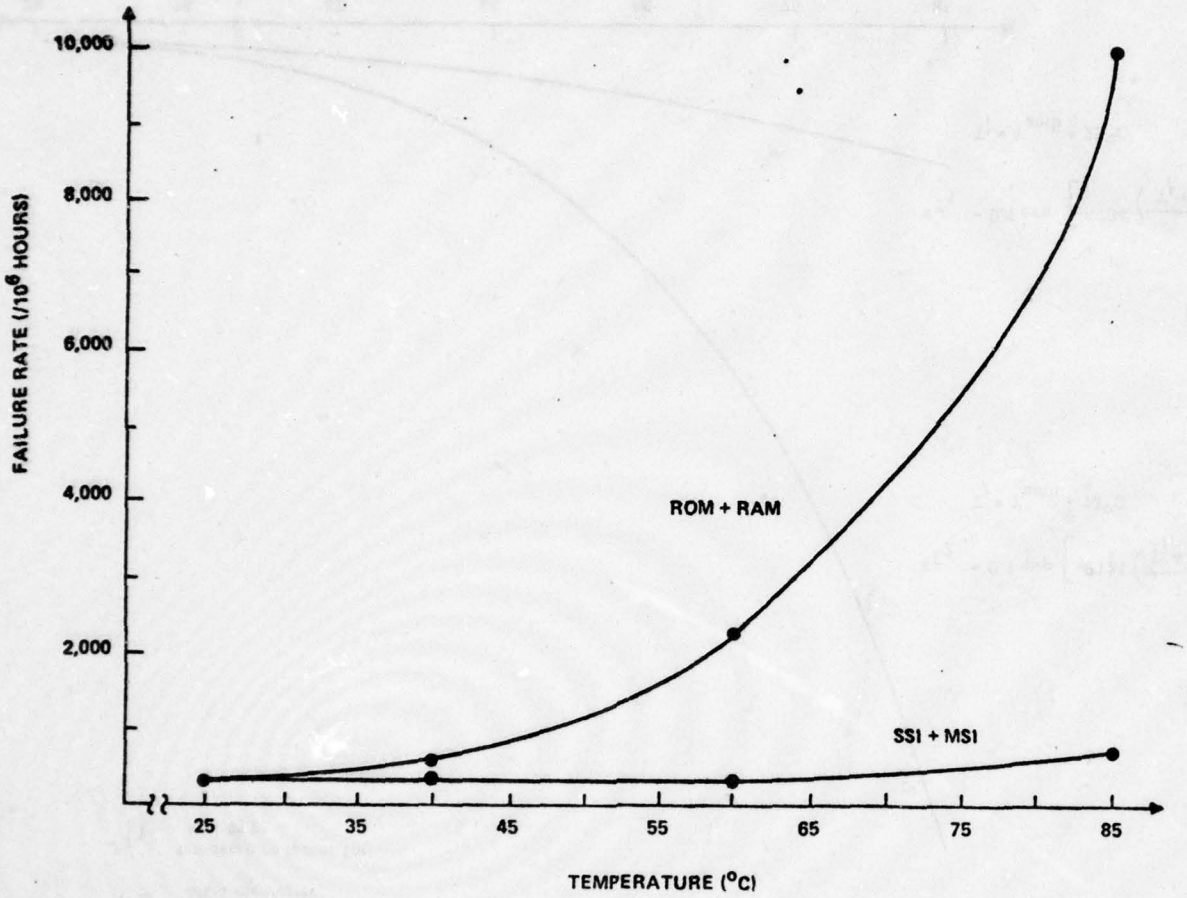


Figure 5.2 Failure Rate As A Function Of Temperature For The PDP 11/70

for use in commercial environments. To summarize the data in the following table, one can estimate that in a computer system (with peripherals not included) 60% of the failures will be in the memory, 30% will be in the CPU and 10% will be in the power supply.

The computer systems that were examined include a PDP-10 with a 256K memory, a PDP-11/40 with 28K memory, an LSI-11 with 28K memory and two multiprocessors at CMU the C.mmp and the Cm*. These computers represent a broad range of computer applications. The PDP-10 is an example of a large time-sharing machine, the PDP-11/40 is an example of a typical minicomputer, and the LSI-11 represents a microcomputer. The C.mmp has 16 interconnected PDP-11/40 processors and a total core memory capacity of one million words. The Cm* multiprocessor has eight LSI-11 processors each with 28K words of semiconductor memory. The individual data is shown in Table 5.3. [22]

5.5 Conclusion and Recommendations for BIT Resource Allocation

The area that is most likely to fail is the logical place for built-in-test capability. It has been shown that at high temperatures memory module reliability degrades to a great extent and dominates the failure rate of all other areas. It is, therefore, logical to provide error-correcting hardware for the memory modules to increase the MTBF of the entire computer system. Error-correcting hardware is not BIT in the strictest sense, but error-correction directly affects maintainability and maintainability is what BIT is all about. A complete discussion of the recommended BIT for memory is given in Section 6.1.

The area that is next most prone to failure is the CPU. The organization and function of the CPU is not simple, which implies that the BIT techniques will not be simple. The CPU performs many functions which require a variety of BIT techniques to provide a BIT capability that is both inexpensive and effective. The complete recommendation of BIT techniques for the CPU is given in Section 6.2.

TABLE 5.3. FAILURE RATES FOR VARIOUS COMPUTER SYSTEMS

System	Failure Rate /10 Hours		% Of Total FR	
PDP-10				
Processor	3156		27	
Memory (256K)	6658		58	
RP-10 Disk Controller	625		5	
Two DF-10 Data Channels	1135		10	
Total	11580		100	
PDP-11/40				
Processor	57		30	
Memory (28K)	108		57	
Power Supply	25		13	
Total	190		100	
LSI-11				
Processor	67		27	
Memory (28K)	154		63	
Power Supply	25		10	
Total	246		100	
C.mmp				
Processors	1008		18	
Memory (1000K)	3904		65	
Switch	202		3	
Power Supply	800		13	
Total	5994		99	
Cm*				
Processors and 32 Memory	880		33	
Memory (192K)	896		33	
Other	656		24	
Power Supplies	250		9	
All of Memory		1392		52
Total	2682		99	

5.6 Reliability Impact of Chassis Level BIT Module

In an attempt to quantify the impact on reliability of an added BIT module, an example of such a configuration has been constructed. The model uses a PDP-11/70 minicomputer to represent an MCF chassis, and to this is added an LSI-11 microcomputer to represent a BIT module. The LSI-11 is easily capable of performing all the error detection, error handling, and error reporting tasks that have been discussed previously. The PDP-11/70 is closely related in performance to a single chassis configuration of an MCF computer.

Using the reliability model in MIL-HDBK-217B, the failure rate of each part of this computer system was determined. To perform these calculations, a computer program at Carnegie-Mellon University was used. The printouts of this analysis of a PDP-11/70 with a chassis (console) BIT module is included in Appendix B. To summarize the findings from this analysis, the basic result is that the failure rate of the BIT module (the LSI-11) is only five percent of the total failure rate. The failure rate calculation was repeated at several temperatures between 25°C and 85°C. The result indicated the relative BIT module failure rate changed only slightly in relation to the whole chassis. Another interesting fact that resulted from this analysis is that roughly half of the failure rate of both the PDP-11/70 and the LSI-11 was from the memory. The 11/70 has a 64K word memory and the LSI-11 has a 4K word memory. At elevated temperatures the failure rate of the memory increased more rapidly than the rest of the components, but the BIT module with its memory increased at approximately the same rate as the 11/70.

This analysis has shown that it is possible to provide an effective BIT module to an MCF computer chassis at a cost to the chassis failure rate of only 5%. The single circuit board sized microcomputer that served as an example of BIT module could easily provide the required built-in-test function needed in each chassis.

6.0 RECOMMENDATIONS FOR THE MODULE LEVEL BUILT-IN-TEST FOR THE MCF AN/UYK-41(V) COMPUTER SYSTEM

In this section, built-in-test approaches for the following types of modules have been considered:

1. Memory Subsystem Modules
2. Central Processing Unit Module
3. Bus Modules
4. Input/Output Modules
5. Analog Modules

It should be recalled from Section 5.0 that a large percentage of the system malfunctions are due to failures in the memory. The failures in the CPU and the power converters constitute most of the remaining failures. Thus, it would be most advantageous to concentrate the BIT resources in these modules.

The Memory Subsystem consists of 32K x 36 bit volatile or non-volatile random access memory modules. The memory modules include their own read/write control circuitry. The number and type of modules used in a system would depend on the memory requirements of the application. For the memory modules simple parity and single error correcting, double error detecting codes are discussed.

The Central Processing Unit consists of one CPU3 module for single processor system and two CPU3 modules for a dual processor system. The CPU3 module has been designed to operate in both modes and its prime function is to emulate the AN/UYK-41(V) (PDP-11/70) instruction set. The Bus modules consist of the Bus Extender Module (BEM) and the Bus Interface Module (BIM2). The BEM is used in multiple chassis configuration to extend the MCF bus system for interchassis communications. The BIM2 has been designed to convert the MCF bus to the AN/UYK-41(V) bus (UNIBUS) so that non-MCF peripheral compatible with the UNIBUS may be used on the MCF computer systems.

The Input/Output (I/O) modules are used to interface the MCF computer system with external devices. The ITEK documentation does not as yet

provide detailed specifications for the I/O modules. However, it is assumed that there will be several different types of I/O modules depending on the interfacing requirements of the external devices.

The CPU3 and the BIM2 are among the most complex modules in the MCF computer system. They perform several interdependent functions. Most of these functions require generations of critical timing and control signals. Also, all of the above mentioned modules perform, as a part of their overall functions, interactive communication among themselves as well as other MCF modules. Due to this variety, complexity and interdependence of the functions in these modules, no single BIT approach can be used to provide a substantial fault coverage. Rather, a set of BIT approaches must be used.

The analog modules in the MCF computer system are the Power Converter Modules (PCM) and the Fan Assembly. The built-in-tests for the analog modules require a different approach. For the analog modules, the types of parameters to be monitored, such as the output voltages, environmental, and thermal and mechanical parameters, are discussed. Alternative ways to implement the BIT hardware on the analog modules is also presented.

For the MCF computer systems, three levels of built-in-tests (system, chassis, and module levels) have been discussed in Section 4.0. Although these three levels of built-in-test have their own respective responsibilities, there is some degree of interaction among them, and as such they cannot be treated as three entirely different approaches.

The BIT approach discussed here for the above mentioned modules pertains mainly to the module level built-in-tests. The module level BIT consists mainly of those testing techniques that require additional BIT circuitry (hardware, firmware) resident on the modules. The main purpose of this additional BIT circuitry is to monitor (detect) and to aid in diagnosing (isolating) hardware faults. These hardware faults may be within the module or in the intermodule communications paths via the system bus. These fault detection and isolation functions of the module level BIT are discussed in this section.

In addition to the fault detection and isolation functions, the responsibility of module level BIT include fault indication, logging, and

reporting. These aspects of module level BIT have not been considered here at this time.

At the module level, the overall approach for analyzing the BIT requirements is as follows:

1. Partition the hardware on the module by functions. These functions should be as loosely coupled as possible. Tightly coupled (or interdependent) functions make fault detection and isolation more difficult.
2. Begin with the most basic (lowest level, innermost) function.
   (a) Determine techniques to test that function with adequate fault coverage making maximum use of internal observability of signals.
   (b) If 2(a) is not possible or fault coverage is inadequate, determine ways of providing functional duplication for the whole or a part of the function as a means for testing.
   (c) If either 2(a)/2(b) are not feasible or external testing of the module functions is desirable, provide externally accessible test mechanism. This may vary from simple test points to read/write maintenance registers. The purpose of this is to increase the observability and controllability of internal signals.
3. Repeat Step 2 with increasing higher level functions (those dependent on the basic functions for their operation). This way maximizes the use of the building block approach to testing. The more basic functions can, if working properly, be used for testing higher level functions.

In view of the above mentioned approach for analyzing the BIT requirements at the module level and the overall MCF BIT requirements discussed in earlier sections, the built-in-test features for the memory, CPU3, BEM, BIM2, I/O and analog modules are described in the following sections.

6.1 Memory Modules

Within the class of memory modules there are volatile and non-volatile types. The volatile type using semiconductor random access memories will be discussed first. Before the various approaches are discussed some background information on reliability assumptions will be given.

6.1.1 Volatile RAM

A block diagram of a memory module with error correction is shown in Figure 6.1. It identifies the parts that have been added to provide the BIT capability. From MIL-HDBK-217B the appropriate failure model is of the form:

$$R = e^{-\lambda t}$$

where: R is the reliability
λ is the failure rate, usually expressed in failures /10^6 hours
t is time, usually expressed in hours

For a non-error-correcting group of electronics, the system reliability is the product of all the reliabilities of the components. This is more easily computed by simply adding the failure rates of the components. However, this method is not applicable to designs that have at least some degree of fault tolerance built into them. In the case of memories built with a single error correcting code, an equation of the following form is correct:

$$R = \left[ke^{-(k-1)\lambda_i t} - (k-1)e^{-k\lambda_i t}\right]^w e^{-\lambda_c t}$$

where: R is the reliability of the system
k is total number of bits in the word
λ_i is the failure rate of a memory chip
λ_c is the failure rate of the control circuitry
t is time
w is the number of sets of chips in the system

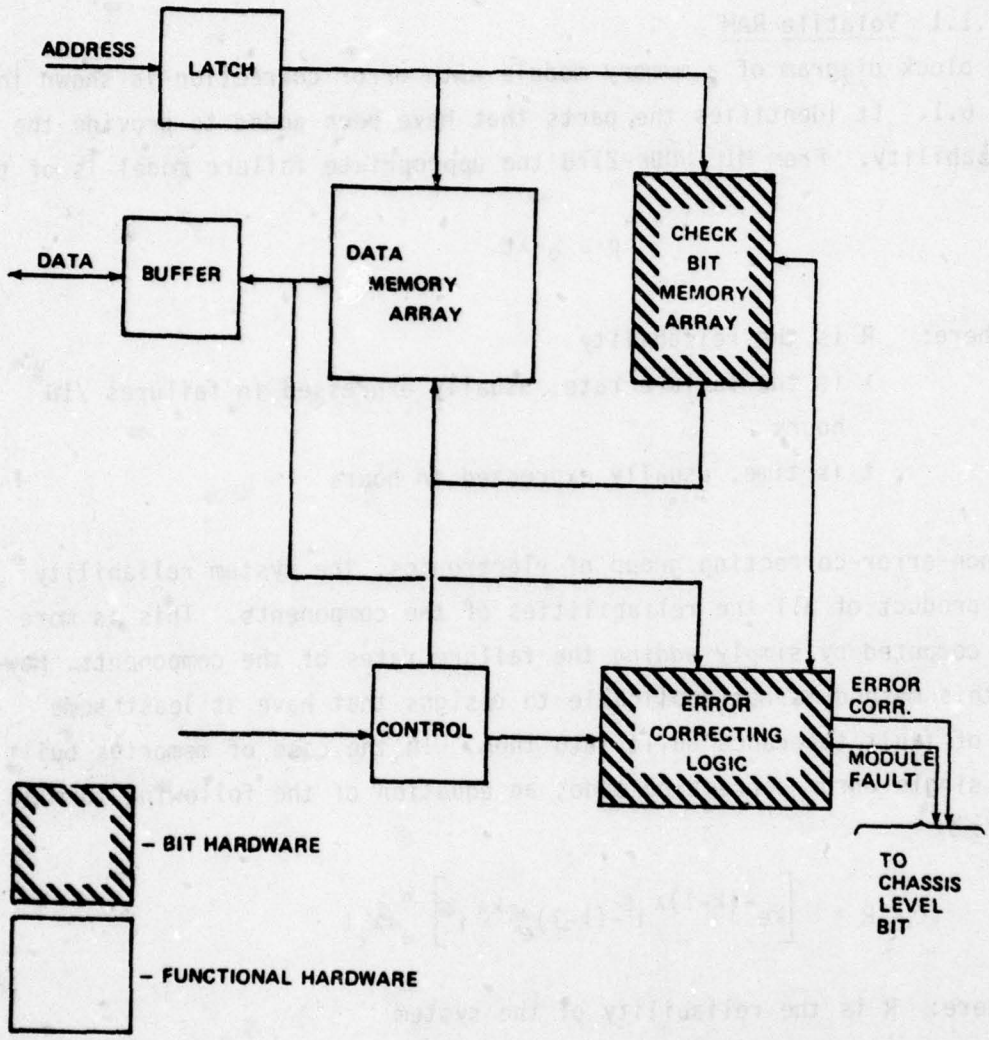


Figure 6.1 Block Diagram of Memory Module with Error Correction

The parameter w is computed by dividing the number of bits on a chip by the number of words on the memory module. A chip organization one bit wide has been assumed. This model also assumes a very pessimistic view, i.e. that of the whole chip failure model. That is, every failure within the chip disables the entire chip. In reality, most of failures within a chip affect only one cell. With the above model, a failure rate (FR) is defined as below:

$$MTBF = \int_0^\infty R(t)dt$$

$$FR = \frac{1}{MTBF} \text{ and,}$$

Based on these assumptions, the suggested BIT approach for the volatile memory module will be a single error correcting code with double error detection. Although the added BIT circuitry is a greater than the 10-20% goal, the reliability is not decreased a similar amount. In fact, the reliability will be significantly increased. The exact increase in the number of packages depends on the size of the memory chips used. Larger chips (16K dynamic RAM) are generally cheaper per bit, more reliable, use less power and take up less board space. For these reasons, large chips should be used as soon as they are able to meet military quality control specifications. The following table (Table 6.1) illustrates the impact on failure rate for various implementations. It is based on a bare bones memory module with 32K words each having 16 bits of data. Because of control circuitry differences in the final MCF implementation, the actual cost and benefit numbers may be slightly different than those listed in Table 6.1. The recommended BIT will store an additional six bits with every data word.

TABLE 6.1. VOLATILE MEMORY MODULE BIT APPROACHES

BIT Method	Chip Size	Chip Type	Estimated Number of Chips in Module	Module Failure Rate (10^{-6} hours)	Module MTBF (hours)
Parity	4K	static	161	489	2040
ECC	4K	static	219	139	7170
Parity	16K	dynamic	61	287	3480
ECC	16K	dynamic	92	141	7060

The data in Table 6.1 shows that in using 4K static RAM, the error correcting code (ECC) requires 36% more chips than the same module with parity. However, the MTBF has increased 250%! Using 16K RAM's, the ECC requires 50% more chips than the module with parity (but less than half the total number using 4K RAM's) and has MTBF 100% greater. One can also see from this data that with ECC the module reliabilities using 4K and 16K RAM's are nearly the same, even though the module reliability is very different when parity is used. This is because the failure model assumed that the whole chip was inoperable when a failure occured. Since there are more memory cells in a 16K RAM, a total chip failure is much more drastic. If a single cell failure model is used, the module reliability is increased by over an order of magnitude and the reliability of the module with 16K RAM's is higher than one built with 4K RAM's. Using the error correcting code, the error detection coverage is greater than 95%.

The recommended BIT for the volatile RAM will take up a relatively large amount of board space. With the space (and power) limitations of a RAM module from the MCF, and with present technology, it may be impossible to implement the recommended BIT. Recognizing this fact, an alternative BIT technique should be used until tecnology produces more complex integrated circuits. The alternative BIT technique is byte parity. This approach will detect over 95% of the faults at a cost of only about 12%.

6.1.2 Non-Volatile RAM

Non-volatile memories use ferrite cores to store the digital data. Since MIL-HDBK-217B does not give any reliability data on ferrite cores, it is not possible to do an analysis to quantify the reliability impact of any BIT technique. However, the volatile RAM provides the same function as the nonvolatile RAM. Therefore, one can reasonably assume that any particular BIT approach would increase the hardware approximately the same amount on each type RAM. Core memories have become a mature technology that has been developed over many decades. This has increased its reliability and reduced its size and cost. Indeed, core memories are more reliable than the semiconductor ones. These reasons would indicate that the use of ECC would be a needless expense.

The recommended BIT technique for the non-volatile memory module will be byte parity. This will detect over 95% of the faults, but will increase cost only by about 12%. However, in the future, it may be desirable to use an error-correction technique on these memories also. Applications are requiring larger and larger memory arrays and the need for long MTBF times is increasing. If the MCF computers are going to use memory arrays near 200K words, then an error-correcting code will be needed on the non-volatile memory. This will be the only way to have a large system that will achieve an adequate MTBF.

6.2 CPU3 Module

The block diagram of the CPU3 module and the Basic Processor as defined in the ITEK F^3 specifications EL-CP-2817-MCF [23] are given in the Figures 6.2 and 6.3, respectively. From these block diagrams a natural partitioning of the CPU3 module is as follows.

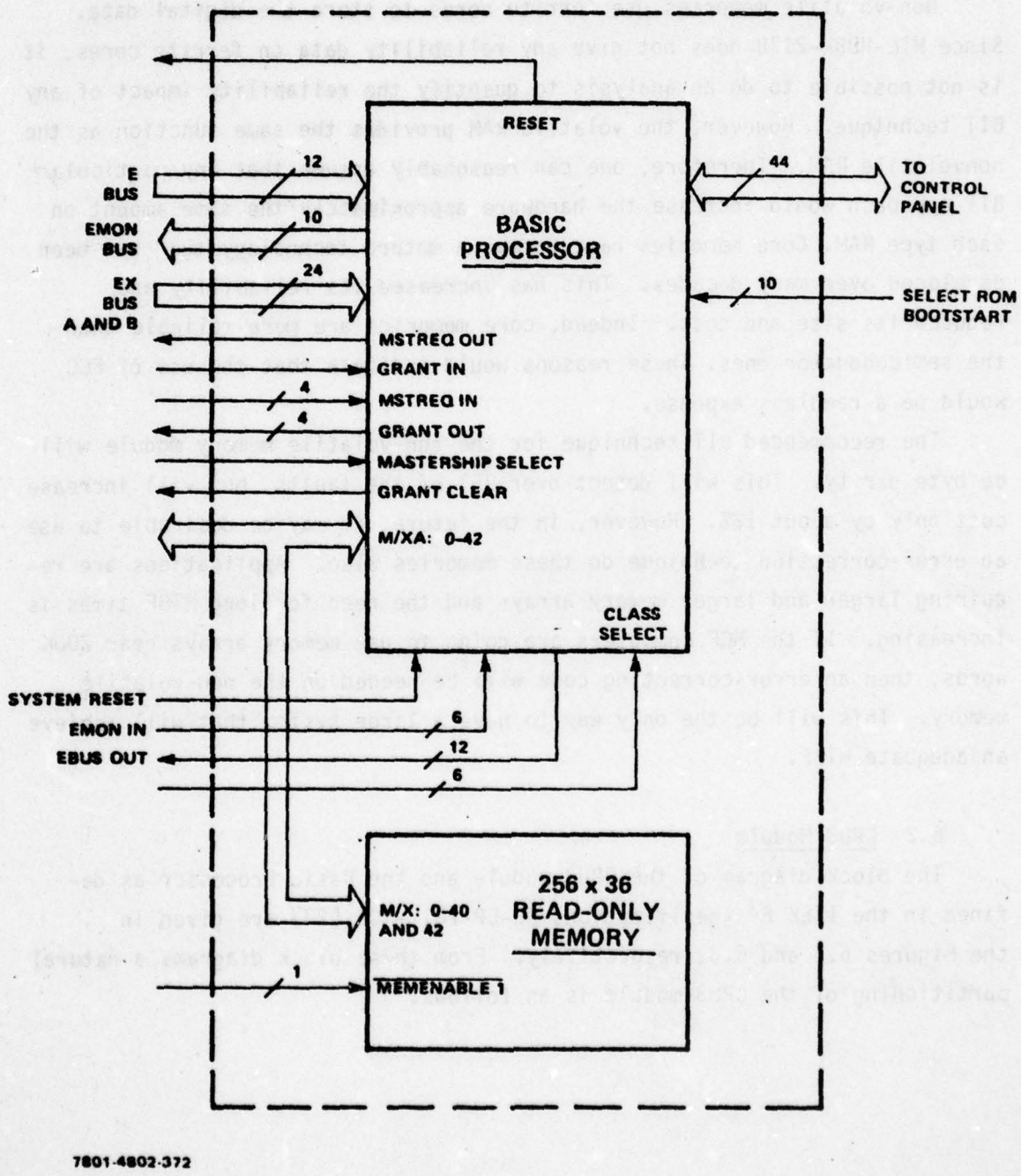


Figure 6.2. CPU Block Diagram [23]

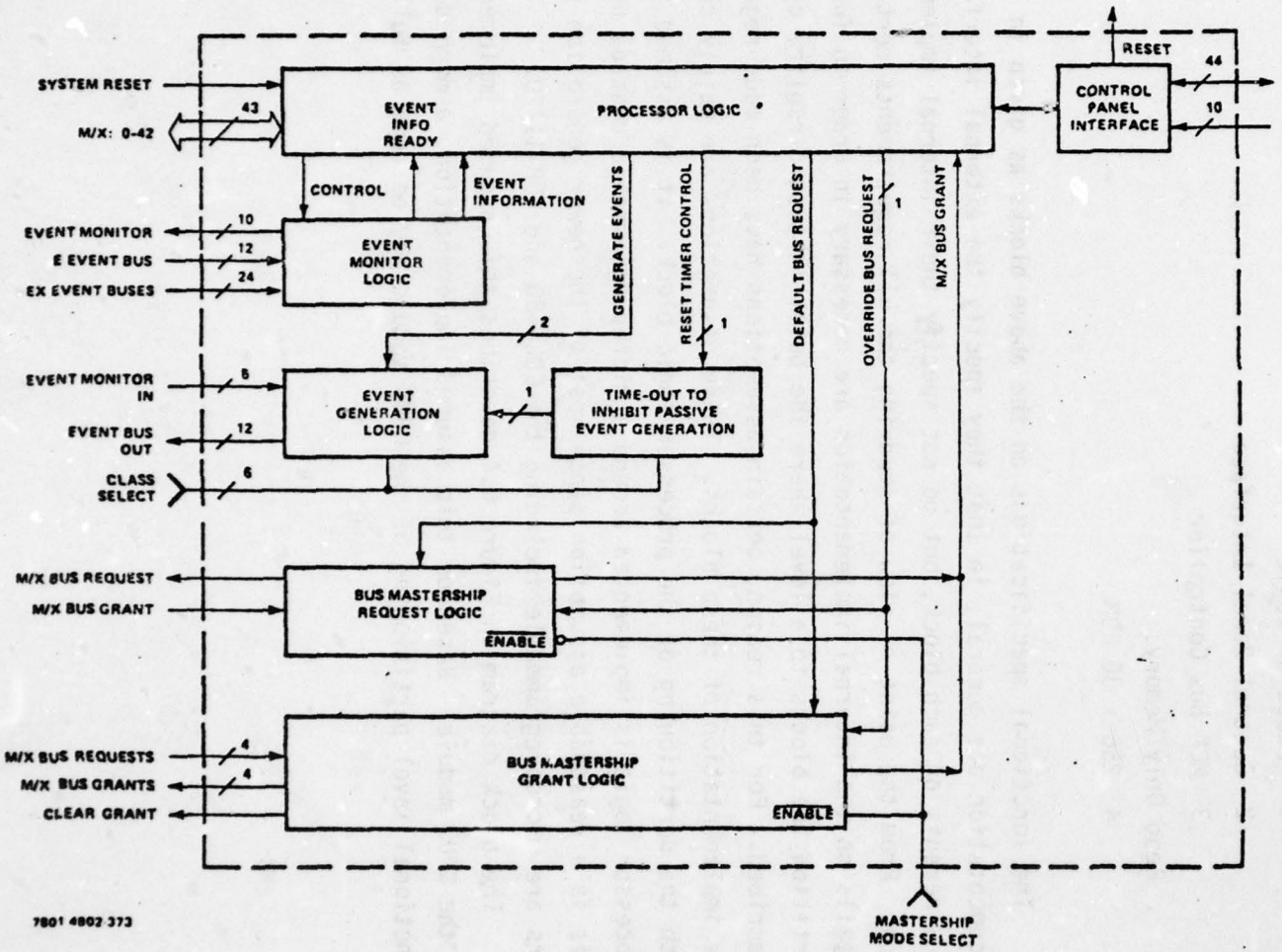
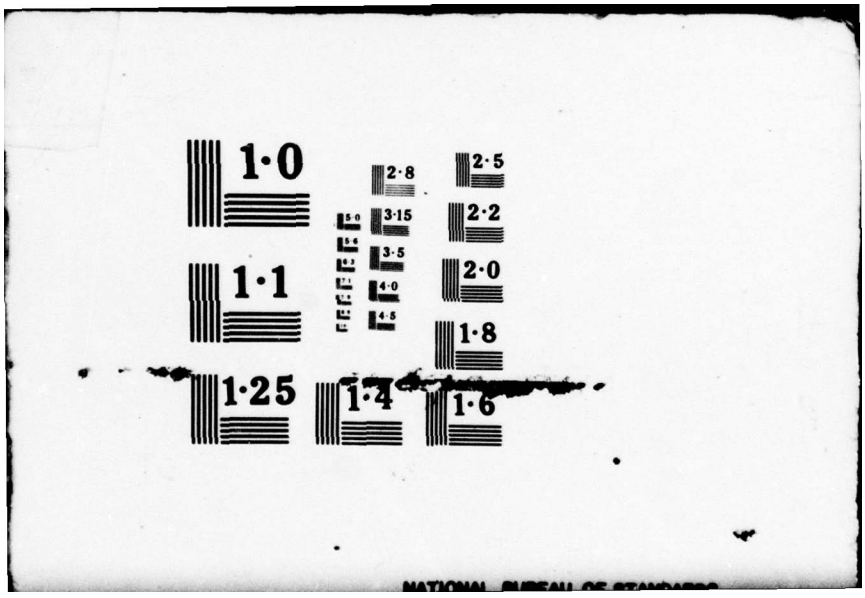


Figure 6.3. Basic Processor Block Diagram [23]

AD-A067 744 BATTELLE COLUMBUS LABS OHIO F/G 9/2
A PRELIMINARY STUDY OF BUILT-IN-TEST FOR THE MILITARY COMPUTER --ETC(U)
MAR 79 J B CLARY, A JAI, S WEIKEL, R SOEKS DAAG29-76-D-0100
UNCLASSIFIED CORADCOM-76-0100-F NL

2 OF 3
ADA
067744


1·0
1·1
1·25
2·8
3·15
3·5
4·0
4·5
1·4
2·5
2·2
2·0
1·8
1·6

CPU3 Module:

Basic Processor Logic

1 Processor Logic

2 Control Panel Interface

3 MCF Bus Controller

Read Only Memory:

4 256 x 36 ROM

The functional specifications on the above blocks as given in the ITEK documentation are general, in that they specify the external interface requirements of each block, but do not specify their internal implementation. From the point of view of studying the BIT requirements certain details on the internal implementation are necessary in order to further partition the blocks to a level where the built-in-test circuitry can be described. For this reason, certain assumptions have been made regarding the implementation of these blocks. These assumptions are mainly concerned with the partitioning of the processor logic block. It is assumed that the processor logic is implemented around a microprogrammable control unit. This is a reasonable assumption since most of the newer generation processors are microprogrammable including the CDC-480 and PDP-11/70.

The block diagram in Figure 6.4 describes this assumed implementation of the CPU3 module. Based on this assumed implementation, a more detailed functional level partitioning of the CPU3 module may be done as follows.

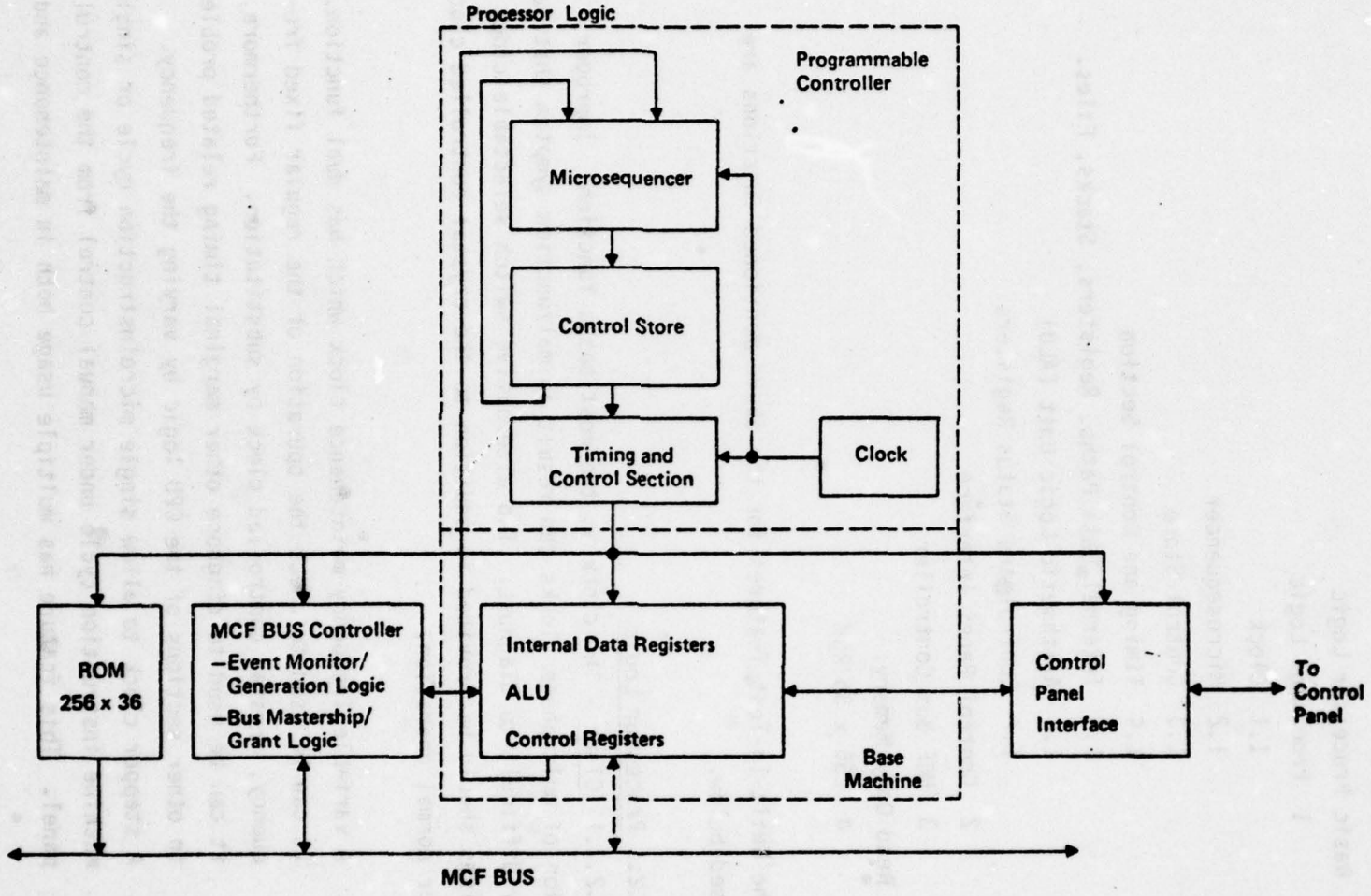


Figure 6.4 Assumed CPU3 Module Implementation Block Diagram

CPU3 Module:

Basic Processor Logic

1 Processor Logic

1.1 Clock

1.2 Microsequencer

1.3 Control Store

1.4 Timing and Control Section

1.5 Internal Data Paths, Registers, Stacks, Files.

1.6 Arithmetic Logic Unit (ALU)

1.7 Control and Status Registers

2 Control Panel Interface

3 MCF Bus Controller

Read Only Memory:

4 256 x 36 ROM

The Built-In-Test features for the above mentioned functions are discussed below.

6.2.1 Processor Logic

6.2.1.1 Clock - The clock is the most basic function. Improper operation of multiphase clocks can result in malfunction symptom that may be very difficult to diagnose. Two alternative switch selectable clock mechanisms should be provided in addition to the crystal controlled clock used for normal operation.

A. A variable frequency maintenance clock which has dual function. It can be used to check the operation of the regular fixed frequency, crystal controlled clock by substitution. Furthermore, it can be used to diagnose other marginal timing related problems in other sections of the CPU logic by varying the frequency.

B. A stepper clock to allow single microinstruction cycle or single machine instruction cycle under manual control from the control panel. This feature has multiple usage both in maintenance and

software development. Its usefulness is limited only by the user accessability of the internal registers after each step.

6.2.1.2 Microsequencer - The microsequencer typically consists of microinstruction register (μIR), microprogram counter (μPC), microaddress register (μADR), microstack registers (μStack) condition code multiplexer, and next address generation logic. This section forms the heart of the base machine control and its failures are also very hard to diagnose. The following built-in-test features are recommended.

A. Parity on all internal registers if feasible.
B. Additional circuitry should be designed into the microsequencer logic to support microstep, microbreak, microrepeat, microaddress set up from the system control panel. These features would facilitate the troubleshooting of the microsequencer logic by stepping through or looping on certain sections of the microcode.
C. The microop-code field in the μIR should have one or two illegal op-codes that cause microtraps which freeze the contents of micro-PC and suspend further control signal generation to the base machine. This can be used for microinstruction retry or branching to microdiagnostic routines. Errors from a parity check on the control store should also cause a microtrap.

6.2.1.3 Control Store - Control store is typically a high speed ROM. The number of microwords and number of bit/microword, of the control store depends on the complexity of the base machine and the microprogramming technique. Horizontally microprogrammed machines utilize fewer words which have longer number of bits. Vertically microprogrammed machines on the other hand have more words with less number of bits per word. In either case, 20,000-50,000 bits of storage is fairly typical. Significant portion of the CPU failure can be attributed to failure in the control store.

Due to large number of bits per word and the higher cost of high speed ROMs, error correction may not be cost effective. Speed consideration may not permit single bit parity on an entire word because of the propagation delays due to multiple stages in the parity generation and checking logic. Preferred approach would be to segment the microword in several fields of 8 to 10 bits and have a parity bit associated with each field. This would increase the control store size by 10 to 12.5%.

Block code correction is another possibility. However, this requires a substantial increase in the BIT circuitry, which is cost effective only if isolation of the failure to the bad bit (or chip) and subsequent error correction using retry mechanism are of importance.

In addition, the size of the control store should be increased to provide space for storing microdiagnostic routines. It should be possible to execute these microdiagnostic in several independent ways. 1) From user written programs by either calls or jumps to the microdiagnostic routines or the execution of certain maintenance instructions. This would allow periodic or idle time testing. 2) From the operator control panel through microaddress load and execute switches. This would allow bypassing the main memory in case it is malfunctioning. 3) Directly from the CPU module with a switch selectable hardware jump to the start of the microdiagnostic routine. (A similar feature is used in the PDP-11/60 diagnostic control store option.) This feature allows bypassing the control panel in case it is malfunctioning.

6.2.1.4 Timing and Control Section - The timing and control signals (levels or pulses) are typically generated by judiciously combining the contents of the microword register with the various phases of the clock pulses. Basically, a section consists of and/or logic which may be distributed across the entire CPU module. For this reason functional testing of this logic is very difficult.

Duplication of this section of logic is a possibility. However, this approach may not be cost effective. Preferred approach is to associate this portion of the CPU logic with the operation of the base machine. The

timing and control signals generated by this section result in operations such as load, shift, rotate the base machine registers, enable/disable data path multiplexers, and select ALU operations, etc. Emphasis should, therefore, be placed on verifying the base machine operations.

Another possibility is to provide as many test points as possible for measurements of the timing and control signals using external test equipment.

6.2.1.5 Internal Data Paths, Registers, Stacks, Files - This section forms the base machine which interacts with all other modules via the MCF bus. It fetches instructions and data from the memory, processes them and outputs the results. During this process, the addresses, instructions, and data are stored in intermediate registers such as the program counter (PC), instruction register (IR), bus address register (BA), general purpose registers (GR) and bus registers (BR), etc.

The preferred approach here is to provide parity on all such internal registers where it is possible.

The registers in the AN/UYK-41(V) would normally be 8, 16 or 32 bits wide. A parity bit may be either associated with an 8 bit byte or a 16 bit word. The former with odd parity is recommended in order to remain compatible with the four bit parity byte provided for the 32 bit address and data information on the MCF M(X) buses. Typically, most of the data registers are fed through the ALU even for simple instructions such as the "move" instruction. In such a case, a parity check before the ALU and a parity generation after the ALU would be the most cost effective to implement the parity tests.

Parity bits (four) must, of course, be generated and checked for the M(X) bus address and data transfers as per the ITEK MCF bus specifications EL-CG-2808-MCF, [24].

6.2.1.6 Arithmetic Logic Unit - ALUs are typically implemented with LSI chips which perform a wide range of functions. Therefore, it is not possible to further partition the ALU functions for built-in-test purposes.

A residue arithmetic coding technique may be used to check most of the ALU functions. Residue codes implemented as separate codes do not interfere with normal ALU operation. The residue generators operate independently on the two inputs and the output of the ALU, as shown in Figure 6.5

Another alternative is to duplicate the ALU logic and detect failures by comparison. This obviously will result in more than 100% increase in hardware cost.

A third alternative is to check the ALU functions using periodic micro or macrodiagnostic routines. The additional cost here is to some extent in additional firmware (or software), but more significantly, it is in terms of system performance degradation due to the CPU time lost in executing the diagnostics.

6.2.1.7 Control and Status Registers - The contents (bits) of these registers, unlike that of the data registers, are generally neither set simultaneously nor do they bear any relation to each other. This typically precludes the use of parity checking.

An alternative is to duplicate some or all of these registers and detect faults by comparison. Such duplication as mentioned before results in over 100% increase in the hardware.

The preferred approach is to make all of the control and status registers accessible (loadable and readable) via microinstruction, macro (machine) instructions and also via the control panel. This will facilitate the testing of these registers through microdiagnostics, macrodiagnostics and also manually. This same approach is also desirable for the internal data registers described in Section 6.2.1.6. This facility also has an important use in software development and debugging.

6.2.2 Control Panel Interface - The main function of the control panel is to allow the user to operate the machine. A second function of the control panel is to provide the operator a certain degree of access and control of the internal hardware of the machine, such as load and read

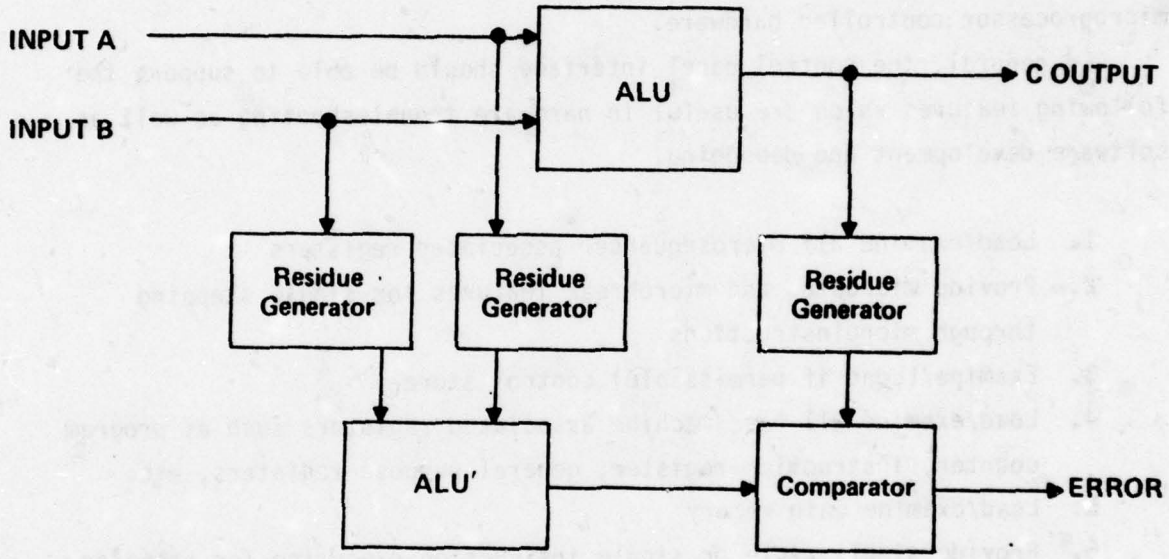


Figure 6.5 ALU Checker

internal registers. This facilitates to a limited extent manual, on-site fault diagnosis in off-line mode.

A third function of the control panel is to aid in performing off-line fault diagnosis from remcte locations. This concept called "Remote Diagnosis" is becoming increasingly popular with commercial machines. The control panel is connected to remote test center via modems or other communication facility. Automatic or manual fault diagnosis can then be done from the remote test center. In order to support such remote diagnosis features, the control panel interface would probably require an intelligent, microprocessor controlled hardware.

In general, the control panel interface should be able to support the following features which are useful in hardware troubleshooting as well as software development and debugging.

1. Load/examine all microsequencer associated registers
2. Provide microstep and microbreak features for single stepping through microinstructions
3. Examine/(Load if permissible) control store
4. Load/examine all base machine associated registers such as program counter, instruction register, general purpose registers, etc.
5. Load/examine main memory
6. Provide single cycle or single instruction execution for stepping through machine instructions.

6.2.3 MCF Bus Controller - There are two buses to be controlled. They are the M(X) bus and the Event bus. The CPU3 module accesses these buses in the same manner as any other module via the event generation logic for the Event bus and the bus mastership request logic for the M(X) bus. In addition, the CPU3 module also contains hardware circuitry to monitor the events on the Event bus and act as an arbitrator for the M(X) bus through the bus mastership grant logic. These functions like those of the timing and control section are indeed difficult to test.

A general testing scheme is to provide time-out circuits for all communication signals that use the handshake protocol. Any time a bus request is issued but not acknowledged within a predetermined time frame, should be indicated as an error condition. This bus time-out error could be as a result of the controller circuitry malfunctioning, or error in the bus (backplane) or due to an absent/malfunctioning external device.

6.2.4 Read Only Memory - This 256 x 36 bit ROM has already been provided with four parity bits (1 parity bit/8 bit byte) as per the ITEK specifications EL-CP-2817 [23]. These four parity bits are adequate for this type of ROM.

6.3 BUS Modules

6.3.1 Bus Extender Module (BEM)

The block diagram of the BEM as defined in the ITEK F^3 specifications EL-CP-2824-MCF [25] is given in Figure 6.6. The function of this module is to provide proper conversion between the MCF buses internal and external to the chassis. This is implemented by a pair of line drivers and line receivers for each signal on the MCF bus as shown in Figure 6.7. The transceiver control circuit determines and controls the proper direction of the signal flow.

The following Built-In-Test features are recommended.

A. Parity check on all groups of signals, such as address and data lines, where parity information has been generated by the source module. If on-line fault isolation to the BEM is important, then the parity check should be performed on both sides of the transceiver. Otherwise, parity check on just one side would be sufficient. In the latter case it would would be more advantageous to apply the parity check after the line receiver shown in Figure 6.7. This would allow parity check on signals on the internal chassis bus lines that have passed through both the line driver and line receiver.

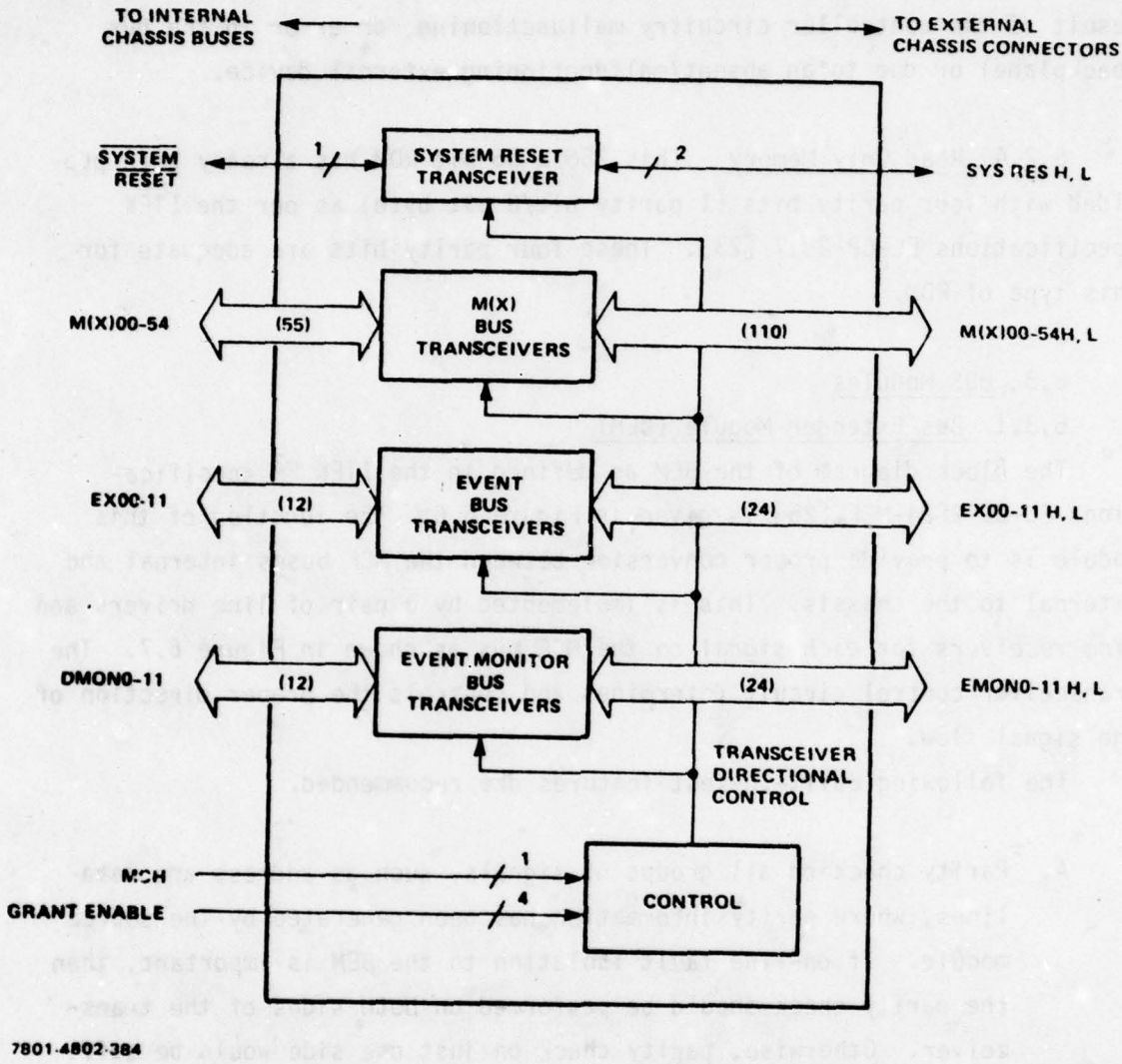


Figure 6.6. BEM Block Diagram [25]

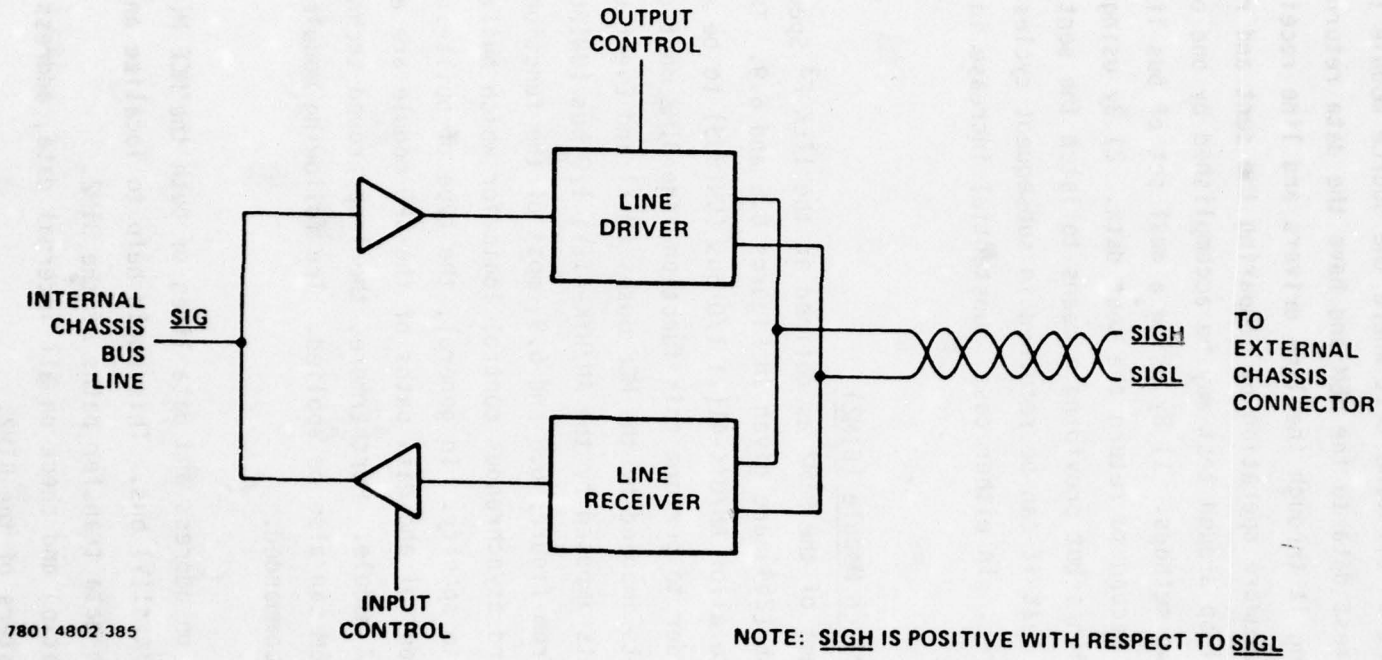


Figure 6.7. BEM Transceiver [25]

B. Loop around of signals on the bus back to the source module. This would support an off-line test where the source module (e.g. CPU) could send test data to the BEM and have the data returned to it after passing it through the line drivers and line receivers. Then test hardware operation by comparing the sent and received data. The loop around test may be accomplished by one of the following two methods. 1) By using a dual set of bus lines, one to send and second to return the test data. 2) By using a single set of bus lines but providing a means to latch the sent data in the BEM, so that it can be returned in subsequent cycles over the same bus wires. In either case, substantial increase in hardware is required.

6.3.2 Bus Interface Module (BIM2)

The block diagrams of the BIM2 as defined in the ITEK F^3 Specifications EL-CP-2828-MCF [264] are given in Figures 6.8 and 6.9. The function of the BIM2 is to allow AN/UYK-41(V) I/O bus (UNIBUS) to be emulated by an MCF CPU. In order to perform this function, the BIM2 must coordinate the timing requirements imposed by the MCF buses (M(X) and Event buses) and the timing requirements imposed by the AN/UYK-41(V) I/O bus (UNIBUS).

As can be seen from figures 6.8 and 6.9, most of the functions of BIM2 require synchronous and asynchronous control logic for which built-in-tests are indeed difficult to specify. In general, the type of built-in-tests recommended for the control and data paths of the CPU module are also applicable to the BIM2 module. Furthermore, the loop around technique recommended for the BEM can also be applied. The following module level built-in-tests are recommended.

A. Parity check on address and data lines of both the MCF M(X) bus and the AN/UYK-41(V) bus. This would help to localize any problems with the data transfer paths of the BIM2.
B. Parity generation and check on all internal data, address and mapping registers of the BIM2.

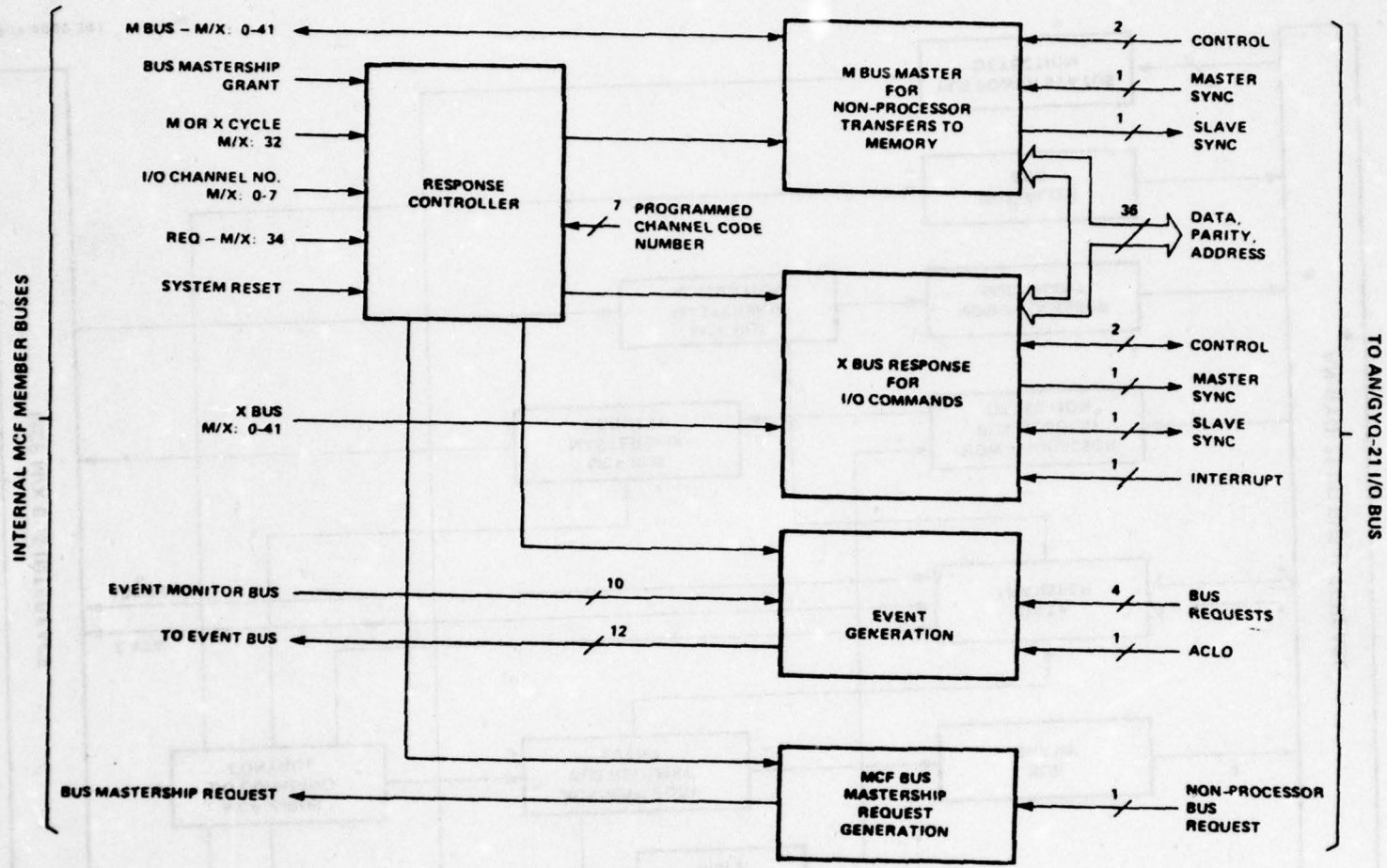


Figure 6.8. BIM2 Control [26]

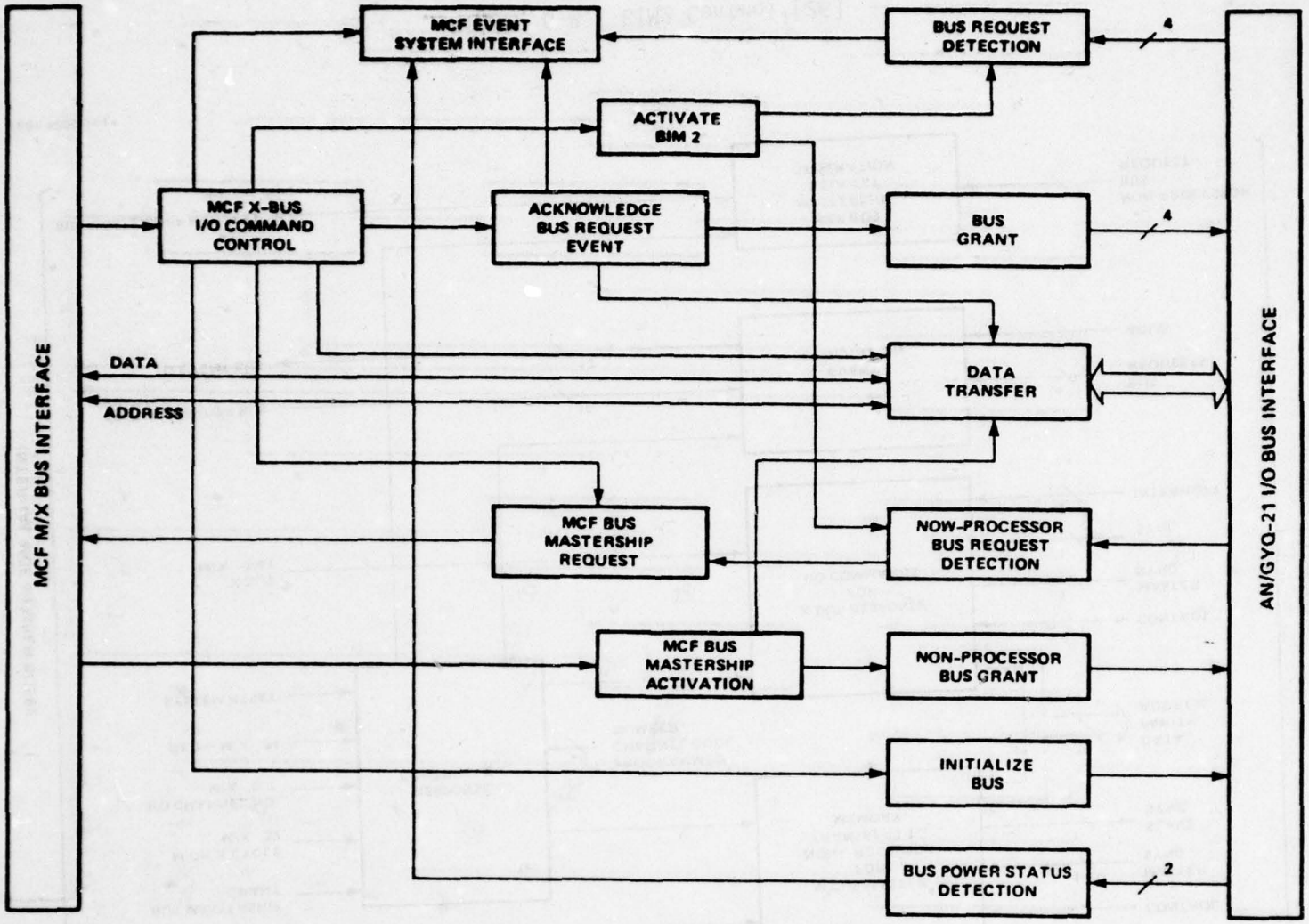


Figure 6.9. BIM2 Function Block Diagram [26]

C. Provide capability to access (load and read) all internal control and status registers via I/O instructions from the CPU.

D. Provide timeout circuits on all communication signals that use the handshake protocol for both the MCF and AN/UYK-41(V) buses.

E. Provide latches on the MCF bus interface of BIM2 to allow loop around of the data sent from the CPU to the BIM2. This would check the MCF bus leading to the BIM2 module and the bus receivers on the BIM2 module under the control of the CPU.

6.4 Input/Output Modules

The recommended BIT approach for the Input/Output Expansion chassis will include a module devoted to chassis level fault detection, isolation, and reporting. The module will also provide an interface to the chassis maintenance panel. This module will be almost identical to the BIT module in the memory expansion chassis since it will perform a similar function. This BIT module will be programmable to enable it to perform an off-line, stand-alone test of all the modules in the chassis. In addition, it will communicate with the BIT hardware on each I/O module and with the system BI software in the fault isolation/reporting process. This section deals with module level BIT; therefore, chassis BIT will not be explained in detail at this time.

Since no individual I/O modules have yet been specified, it is difficult to recommend specific built-in-test techniques. However, several generally applicable BIT approaches are available to the designer of the I/O module. These concepts, discussed below, should be included in the design stage of these modules. These techniques would provide module level BIT for I/O modules whether the modules are located in an I/O expansion chassis or in a main computer chassis.

6.4.1 Parity - A single parity bit on each eight-bit byte of data should be generated (checked) when it enters (leaves) the MCF bus. In

addition, the use of parity within all I/O modules is recommended as a method to detect errors in the data. It is also recommended to send (check) parity when data is sent (received) out of the MCF I/O expansion chassis. In this way there would be a check on the entire data path from the external I/O device through the cables and I/O module and through the MCF bus system. In addition to data, parity should also be sent with addresses and operation codes where these are sent over the communication buses. The added hardware cost of these BIT approaches would be approximately 15%.

6.4.2 Loop Around - Loop around involves a controlling device sending a particular command to another device which causes the receiving device to send an acknowledge back to the controller. This technique provides the capability to check the bus wiring, connectors, and the receivers/drivers of an I/O module. While this test by itself leaves a major portion of a module unchecked, the functions which are checked are essential to the operation of the module. This communication section must function properly if it is to be tested more completely with software. Successful loop around testing gives a higher confidence level to off-line tests and aids fault localization, particularly in bus faults. The small amount of hardware required to perform this BIT function would consist of a set of multiplexers (or registers) on each I/O module to store the data to retransmit on the bus.

6.4.3 Time-Out - In addition to the time-out checking within the CPU there should be timers within the I/O modules which would detect errors in the control portions of the modules. Control circuitry is in general difficult to test short of duplication. Time-out signals do, however, provide an inexpensive method to detect major faults in most control functions.

6.4.4 Replication - For cost reasons, it is not recommended to duplicate each I/O module. However, some critical portions of some modules

may be candidates for duplication. By duplicating only relatively small sections of a module it is possible to keep BIT hardware down to a reasonable level, while providing essential on-line fault detection capability. In addition, it may prove necessary from a reliability viewpoint for some applications to provide TMR (triple modular redundancy) to a few vital control functions. This approach, while expensive, does provide fault tolerant hardware that allows the unit to perform its required function until it is convenient to repair it.

6.5 Built-In-Testing for the MCF Analog Modules

The two major analog modules in the MCF system are the power converter module (PCM) and the Fan assembly. From the most rudimentary point of view, these modules can be tested simply by measuring those output parameters which interface with the remainder of the MCF: output voltage, ripple, regulation, air flow, etc. Because of the analog nature of the PCM and Fan modules, however, these output parameters are strongly influenced by environmental parameters such as operating temperature, line voltage, and load current. As such, if the false alarm rate for the BIT system is to be kept within reasonable bounds one must also measure such environmental factors to determine whether a measured deviation of the system output parameters is due to a failure of the analog module or the environment in which it operates. Finally, high power analog devices such as the PCM and Fan are characterized by thermal and mechanical parameters; transformer and rectifier temperatures, fan vibration, etc., which are indicative of failures not yet manifested in the output parameters. An effective BIT system should, however, measure such parameters as a means for spotting impending system failures thereby preventing costly burnouts.

Given the above observations, rather than simply monitoring a set of output parameters, an effective analog BIT system must be able to compare, extrapolate, and evaluate measured data. As such, some type of "intelligence" is required by the BIT system. Unlike the digital MCF modules the analog modules have no inherent "intelligence" which can be shared with the BIT system. As such, the key to a BIT system for the

analog modules is the inclusion of some type of BIT "brain". The design of the "brain" is the key factor in determining the performance characteristics; time to detect, false alarm rate, etc., of the BIT system with various tradeoffs possible between serial and parallel processors, etc. Several possible organizations for the BIT "brain" are discussed in the following sections along with the performance which can reasonably be expected from each.

Although the inclusion of a BIT "brain" in an analog module may at first seem to be economically prohibitive this is not, in fact, the case. Indeed, given the relative cost of digital to analog devices an entire microprocessor system for the BIT "brain" would not represent a significant percent increase in the cost of either the PCM or Fan. Indeed, the entire cost of the BIT system would be recovered by the prevention of a single major component burnout; fan motor, transformer, etc. Moreover, the BIT system replaces the usual protective circuitry in either the PCM or Fan. As such, only the cost difference represents a true cost increase attributable to BIT.

In the following, several potential BIT "brain" organizations are discussed and the performance to be expected from a typical design is evaluated. The primary parameters in the PCM and Fan modules which should be monitored are tabulated in the following section. This is followed by a description of several BIT "brain" organizations in Section 6.5.2. Section 6.5.3 is devoted to a discussion of the BIT power supply and discusses several techniques for assurance of reliable BIT performance in the face of a failure of its own power supply. Section 6.5.4 is devoted to a discussion of BIT self-test procedures while Section 6.5.5 is devoted to an evaluation of a typical BIT system vis-a-vis its false alarm rate, time-to-detect, percentage of failures detected, and reliability.

6.5.1 What to Measure

As indicated above the PCM and Fan parameters which should be measured by a BIT system may naturally be catagorized into three class: output parameters, environmental parameters, and thermal and mechanical parameters.

Since the time constants associated with these parameters varies from microseconds to seconds they may be further classified into fact, medium and slow categories dependent on the speed with which a failure must be detected. The primary PCM parameters to be monitored are tabulated below.

6.5.1.1 Output Parameters

1. Output voltages: 5.08 ± 0.05 Vdc, -12.05 ± 0.05 Vdc, and 15.10 ± 0.05 Vdc. In addition to monitoring these parameters the BIT system is required to initiate an automatic cut-off sequence when the output voltages reach a critical overvoltage. For this purpose the cut-in limits are 6.3 ± .5 Vdc for the 5 volt line, -14.0 ± .7 Vdc for the -12 volt line, and 16.9 ± .7 Vdc for the 15 volt line. Furthermore, the BIT system must initiate an interrupt to initiate a power-down cycle whenever any of these output voltages reach an undervoltage state of 20 ± 10 percent less than nominal.
2. Air Flow: The flow rate of the MCF Fan module is specified as a function of static pressure, hence, both of these parameters must be measured and compared by the BIT system to verify proper Fan performance.
3. Ripple: This parameter must be less than 100 millivolts on all output lines over the entire operating range of the PCM. Upon failure the BIT system should send an interrupt indicating failure but no shutdown sequence is required.
4. BIT System Voltage: A deviation from nominal by the BIT system voltage should be signaled by an interrupt. Here, the threshold for the failure indication should be set well within the tolerance limits of the BIT system to guarantee correct performance of the BIT system in spite of the failure of its own power supply. Protection of the BIT system power source is discussed in more detail in Section 6.5.3.

6.5.1.2 Environmental Parameters:

1. Line Voltage: 95-130 Vac at 47-440 Hz. Although the PCM and Fan are required to operate over a wide range of line voltages, the actual values of these parameters must be monitored within this range to determine if an observed deviation in the output parameters is, in fact, due to a problem in the line voltage rather than the MCF.
2. Load Current: For the 5 volt line the output current specifications are 8-40A for the PCM1 and 8-65A for the PCM2. For the -12 volt line they are .2-6.5A and .2-13.0A, respectively, and for the 15 volt line they are .2-4.0A and .2-7.0A, respectively. The BIT system should monitor these parameters both for the purpose of distinguishing between PCM failures and load failures and to initiate protective circuitry in the event of overload.
3. Internal Voltages and Currents: It is believed that to minimize false alarms that certain internal PCM voltages and currents should be monitored. In effect, such parameters yield a degree of fault isolation within the PCM. Although it is not our goal to isolate failures beyond the module level, we believe that a certain amount of fault isolation within the module is necessary to prevent false alarms. Indeed, since in an analog system failure detection is unambiguous, false alarm prevention amounts to accurately distinguishing between failrues in a module and failures in its environment (i.e. fault isolation up to the module).

6.5.1.3 Thermal and Mechanical Parameters:

1. Diode Junction Temperature: Since a major cause of power supply failures is diode burnout, the MCF specifications required that diode junction temperatures be monitored with automatic shutdown being initiated whenever they reach critical temperature (146°C). Of course, the BIT system may also employ junction temperature

measurements in a manner analogous to that described above for the internal voltages and currents as an aid in false alarm prevention (fault isolation).

2. Component Temperatures: Although the output parameters of the PCM or Fan module may still be in tolerance, if critical component temperatures including transformer temperature, fan motor temperature, and chassis temperature are out of tolerance a failure or impending failure in the moduel is indicated. As such, these parameters should be monitored.
3. Vibration: As with component temperatures unusual vibration in either a power handling PCM component or the Fan assembly is indicative of system failure and should be reported by the BIT system.
4. Humidity: Since changes in humidity are a good indication of seal integrity in hermetically sealed components (i.e., Xformer and fan motor) which is easily monitored, it is recommended that the PCM and Fan BIT systems include a humidity monitoring capability for such components.
5. Ambient Temperature and Humidity: For the temperature and humidity measurements discussed above to be meaningful it must be compared to ambient values. As with the previously discussed environmental parameters this comparison is necessary to prevent false alarms.

Since the time constants associated with changes in the above vary from microseconds to seconds, the BIT system's handling of these parameters must also vary. For this purpose, the above described parameters are tabulated below in three categories characterizing their time constants as fast, medium or slow. The fast time constant parameters are those whose failure must be detected on a microsecond time scale if damage to the system is to be prevented. The medium time constant category represents parameters whose failure should be detected in a period of milliseconds. These are typically parameters whose failure will not lead to immediate

damage to the system but may cause unreliable operation of the MCF. Finally, the time constants underlying most of the thermal, mechanical, and humidity related parameters are sufficiently long that these parameters need only be monitored on an interval of a second or so.

Fast Parameters:

1. Overvoltage
2. BIT System Voltage
3. Line Voltage
4. Load Current
5. Internal Voltages and Currents

Medium Parameters:

1. Undervoltage
2. Air Flow
3. Ripple
4. Diode Junction Temperatures

Slow Parameters:

1. Component Temperatures
2. Vibration
3. Humidity
4. Ambient Humidity

6.5.2 BIT System Organization

Because of the time constant variations among the parameters which the PCM and Fan BIT systems must monitor, no one organization for the BIT "brain" is immediately obvious. Since the time constants for the fast components are on a par with the cycle speed of a typical microprocessor, a parallel processing scheme is needed for handling these parameters. On the other hand, the time constants for the slow parameters are quite compatible with a sequential processor. These considerations, however, must be

balanced against the computation and comparison of data required to prevent false alarms. As such, we have investigated three potential BIT system organizations in an effort to determine the optimal performance which can be expected from the PCM and Fan BIT systems. These include a parallel processor with minimal computation capability, a microprocessor based serial processor and a hybrid of the two. These are described below together with a comparison of their capabilities.

6.5.2.1 Latches Plus Logic - The simplest and fastest BIT organization investigated is illustrated schematically in Figure 6.10. This parallel processor which we term "latches plus logic": (L + L) is based on an array of latches which sense the various analog system parameters. Whenever a parameter crosses a prespecified threshold, a latch is triggered and sends a binary input to a hard wired logic array which makes a Boolean decision as to whether or not the deviation from nominal by this parameter represents a module failure. If so, the appropriate interrupt or automatic shutdown sequence is initiated.

The main advantage of the L + L organization is the speed with which it can detect the failure of a fast time constant parameter. On the other hand only Boolean information is available to the logic array which may, in turn, make only Boolean decisions. As such, little capability for careful data analysis and false alarm prevention exists.

6.5.2.2 Analog to Digital Converter plus Microprocessor - A second BIT organization made up from an A/D converter and a microprocessor (A/D+μP) is illustrated in Figure 6.11. Here, the analog data is fed into a multichannel A/D converter with the various channels being called sequentially by a microprocessor. The μP then analyzes the data from each channel and compares data from various combinations of channels to detect failures and to determine whether or not there cause is within the given analog MCF module.

The advantage of the A/D+μP Organization is its powerful computational capability which allows it to compare data from several channels and/or to

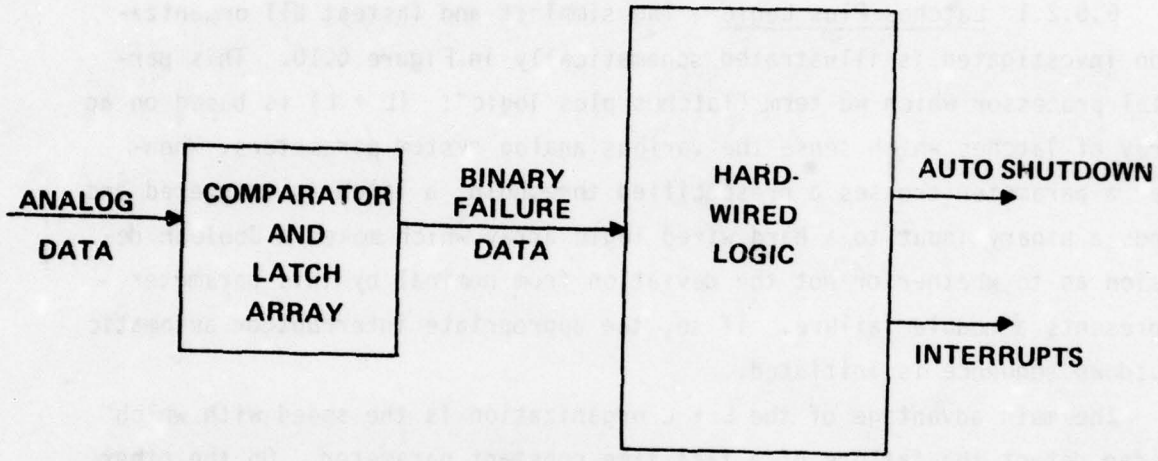


Figure 6.10 Latches Plus Logic Approach

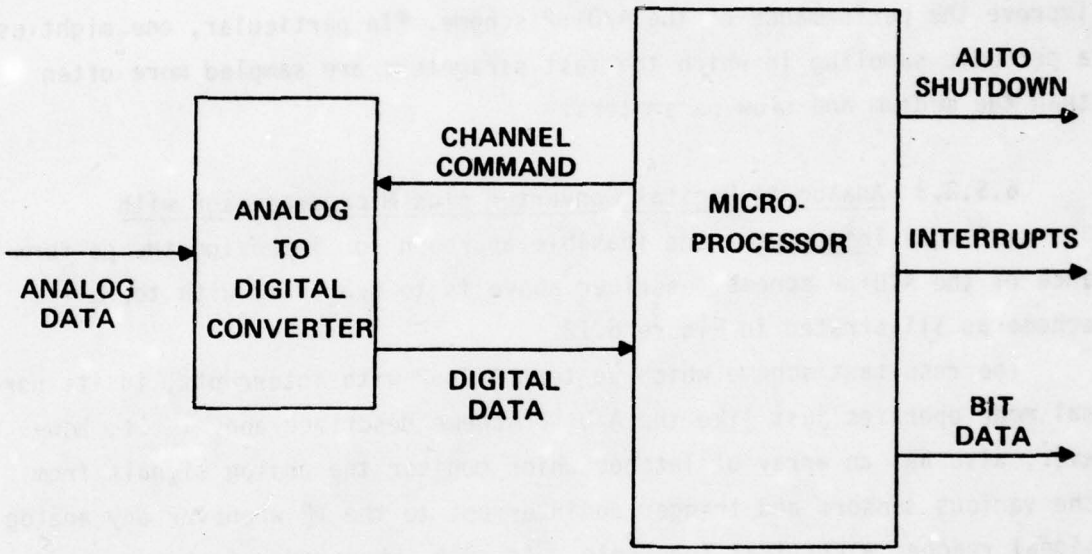


Figure 6.11 Analog-to-Digital Converter Plus Microprocessor

compare data with stored information to determine whether or not a detected failure is internal or external to a given module. As such, the false alarm rate can be minimized with the A/D+μP organization. Unfortunately, given the speed of a typical microprocessor and the sequential nature of the A/D+μP BIT organization, the time interval between the various samples of a given channel may be as large as a millisecond. Since this exceeds the time constant of the fast parameters, this BIT organization may not be acceptable in practice. Of course, several modifications can be made to improve the performance of the A/D+μP scheme. In particular, one might use a periodic sampling in which the fast parameters are sampled more often than the medium and slow parameters.

6.5.2.3 Analog to Digital Converter plus Microprocessor with Interrupt - One feasible approach for improving the performance of the A/D+μP scheme described above is to hybrid it with the L + L scheme as illustrated in Figure 6.12.

The resultant scheme which we term A/D+μP with interrupts, in its normal mode operates just like the A/D+μP scheme described above. It, however, also has an array of latches which monitor the analog signals from the various sensors and trigger an interrupt to the μP whenever any analog signal reaches a critical threshold. As such, whenever a fast parameter crosses its threshold, the μP is called from whatever it is doing to investigate the fast parameter before any catastrophic failure takes place. The scheme, therefore, has the computational power and false alarm prevention capability of the A/D+μP BIT organization with a reaction time comparable to the L + L organization.

A summary of the three proposed BIT organizations and their capabilities vis-a-vis reaction time and false alarm prevention is given in Table 6.2 below.

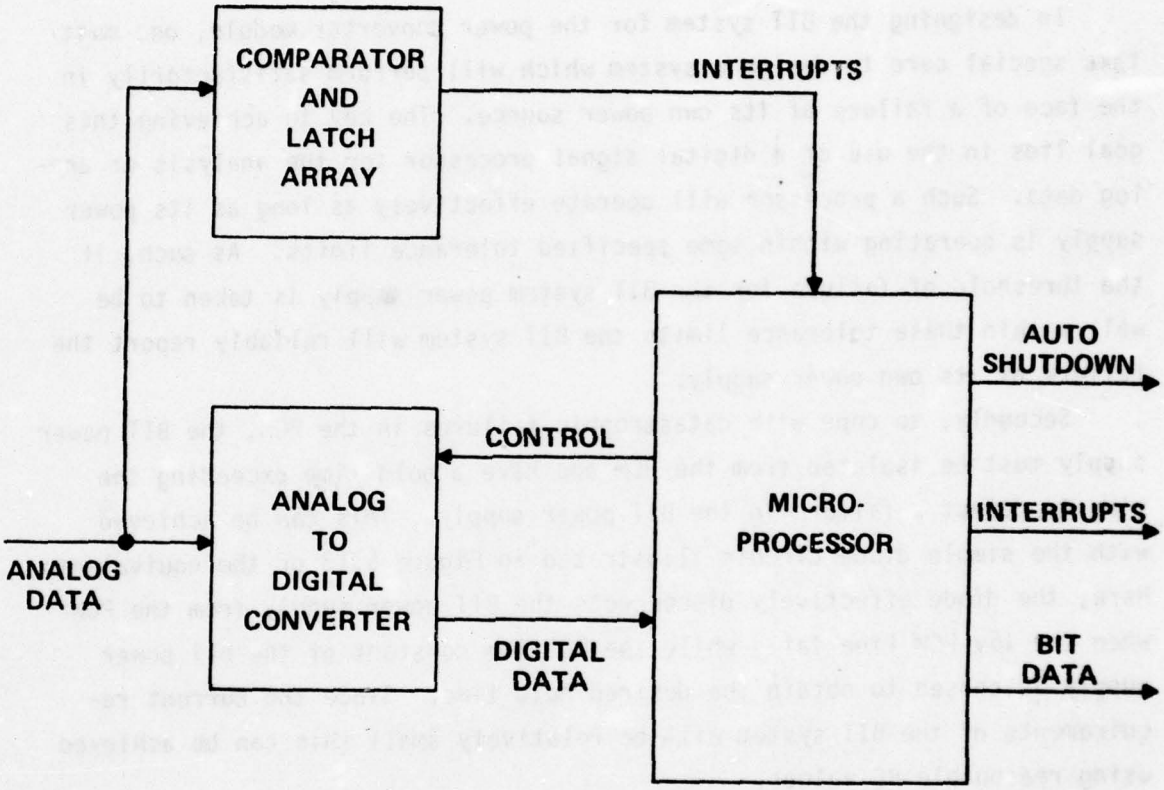


Figure 6.12 Block Diagram Of A/D + μP With Interrupt BIT Organization

TABLE 6.2. PERFORMANCE OF THE THREE PROPOSED BIT ORGANIZATIONS

	L+L	A/D+μP	A/D+μP with Int.
Reaction Time	very fast (1μs)	medium (1ms)	fast (50μs)
False Alarm Prevention	minimal	good	good

6.5.3 The BIT System Power Supply

In designing the BIT system for the power converter module, one must take special care to design a system which will perform satisfactorily in the face of a failure of its own power source. The key to achieving this goal lies in the use of a digital signal processor for the analysis of analog data. Such a processor will operate effectively as long as its power supply is operating within some specified tolerance limits. As such, if the threshold of failure for the BIT system power supply is taken to be well within these tolerance limits the BIT system will reliably report the failure of its own power supply.

Secondly, to cope with catastrophic failures in the PCM, the BIT power supply must be isolated from the PCM and have a hold time exceeding the time to detect a failure in the BIT power supply. This can be achieved with the simple diode circuit illustrated in Figure 6.13 or the equivalent. Here, the diode effectively disconnects the BIT power supply from the PCM when the 15v PCM line fails while the RC time constant of the BIT power supply is chosen to obtain the desired hold time. Since the current requirements of the BIT system will be relatively small this can be achieved using reasonable RC values.

Finally, the display used to indicate PCM failures must be non-volatile so that the failure indication remains after shutdown of the system.

6.5.4 Testing the Tester

As with any test system, one must face the question of testing the tester. For the BIT "brain" one can use standard digital system test algorithms. When a microprocessor is employed, a self test algorithm can be used, either in slack time or periodically programmed into the test algorithm. Alternatively, the MCF itself or one of the other distributed

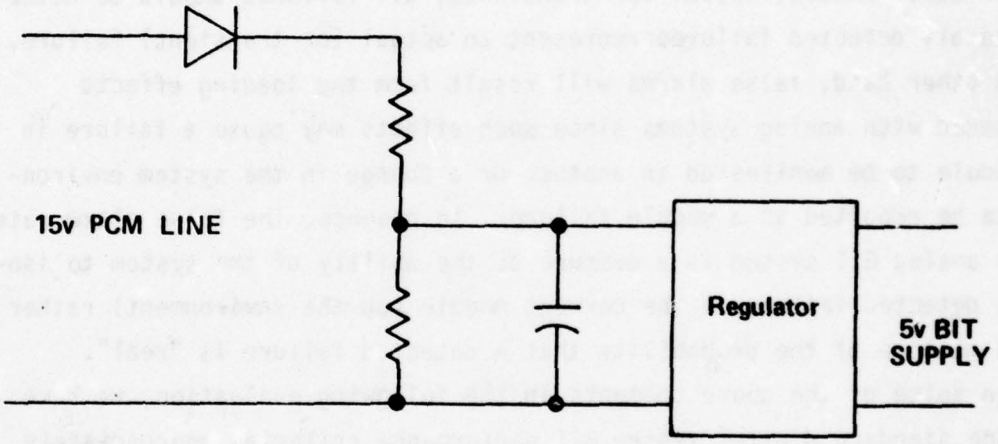


Figure 6.13 Diode Circuit For Isolating The BIT Power Supply From The PCM And Increasing Its Hold Time

processors in the BIT system can be used to test the BIT "brain" in the analog modules.

Secondly, the BIT brain should be programmed to test its own sensors. While an outright determination of sensor accuracy can only be achieved with some type of redundancy, the BIT "brain" can easily spot open and short circuited sensors which represent the majority of sensor failures.

6.5.5 Evaluation of Analog BIT System Performance

For an analog system, the usual measures of test system performance such as percent of failures detected and false alarm rate are somewhat inappropriate. Indeed, except for transients, all failures should be detected and all detected failures represent an actual (or transient) failure. On the other hand, false alarms will result from the loading effects associated with analog systems since such effects may cause a failure in one module to be manifested in another or a change in the system environment to be reported as a module failure. In essence, the false alarm rate for an analog BIT system is a measure of the ability of the system to isolate a detected failure to the correct module (or the environment) rather than a measure of the probability that a detected failure is "real".

In spite of the above comments in the following evaluation, we have used the standard digital system BIT performance criteria, appropriately reinterpreted, to make our evaluation of the PCM and Fan module BIT systems compatible with the evaluations of the digital MCF modules. The evaluation assumes the A/D+μP BIT organization with interrupts implemented with a Mostek F8 microprocessor. Although this is certainly not the ultimate approach or the only implementation, thereof, we feel that its performance is a reasonable benchmark by which the performance of other BIT system organizations and/or implementations may be measured.

Our prototype BIT system for the PCM and Fan modules of the MCF was a recently introduced variation on the F8 (Model 3870) which contains 2K of ROM and 64 Bytes of RAM on the CPU chip, thereby, yielding a single chip μP system. In addition to the μP, a monolithic A/D converter (Teledyne 8703)

and an octal latch (Fairchild 74S373), together with discrete signal and power conditioning components and sensors, make up the BIT system. The performance parameters as they apply to the PCM module are discussed in the next paragraph.

The percent of failures detected will be 100% for the PCM module with BIT. As long as all of the output parameters through which the analog modules interface with the MCF are monitored, all failures will be detected. All detected failures will represent real or transient failures in the MCF or its environment. As indicated above, the false alarm rate in the analog BIT systems is really a measure of the ability to isolate a detected failure to the correct module or the MCF environment. With a full microprocessor in the BIT "brain" and given time to run cross-checks on a detected failure, the false alarm rate can reasonably be kept under 5 percent. Since all computation required for the BIT system can be done by comparison of data taken from one channel with data taken from another and/or stored parameters, the analysis of the data taken from any one channel can be conservatively carried out in 25 cycles of the μP. Given the 2μs cycle time of the F8, with the system programmed to check for interrupts after the analysis of data from each channel, this will result in a time to detect of 50μs. Here, we note that one can tradeoff BIT reaction time and false alarm rate since making more cross-checks to reduce the false alarm rate will increase reaction time and vice-versa. Of course, one does not require fast reaction time for the various medium and slow time constant parameters and can therefore make more cross-checks on these parameters than the fast time constant parameters.

The cost parameters that measure hardware cost (power, space, and failure rate) are discussed in Section 8.0. This module level BIT has no effect on the application programs, but the small impact on diagnostic and operating system software is also discussed in Section 8.0. More detailed information on the cost parameters for all the modules is given in Appendix C.

7.0 ELAPSED TIME MEASUREMENT

The purpose of specifying an elapsed time recorder and indicator on each module is to be able to enforce the MCF warranty concept on a module basis. With such an indicator, it is possible not only to tell if a module has been in use past its warrantied period, but to establish a failure rate distribution as the modules are sent back for repair. This type of information is useful in refining the failure rate model for the modules and identifying batches of unreliable modules. For these reasons, it is desired that the elapsed time indicator show more than whether or not the warranty period is passed. It should show with some degree of accuracy (at least 3%) the actual time the module has been powered on. Two distinct approaches have been considered as candidates for recording this time interval. One is analog and one is digital with each approach having its own set of advantages and disadvantages.

The candidate analog version is a small transparent tube filled with a mercury compound that plates out onto the tube walls when a voltage is applied across the ends of the tube. This tube would be connected to the module's five-volt supply. The amount that has plated onto the wall of the tube will be proportional to the time period that power has been applied to the module. Commercial versions have been used successfully for a number of years and their cost is low (about five dollars). This simple, inexpensive device has a non-volatile display enabling the elapsed time to be read by a serviceman or operator whether the module is in or out of the chassis and with or without power applied.

However, the elapsed time cannot be read at any time by the computer, and to be read by anyone, a cover would probably have to be removed from a computer chassis. Another problem may arise from use in environments that are subject to a high level of shock. That is some of the mercury may become dislodged from the tube, thus giving an erroneous reading.

The alternative is a digital technique utilizing a counter and a non-volatile storage. Since timing components such as crystals and capacitors have a high failure rate as compared with digital logic, it is not desirable to have a self-contained timer on each module. A more reliable approach would be to have a clock in each chassis that would send a timing

signal to all modules within the chassis. This clock should have duplicated timing components so that the timing signal's reliability would be high. On each module there would be a non-volatile storage device such as EAROM (electronically alterable read only memory) or a ROM with fusible links. Some small amount of control circuitry would also be needed to properly code the timing signals into the storage device. To reduce the amount of control circuitry that would need to be added to each module, the central clock generation circuitry should also contain the frequency dividers. Only a pulse per hour or similar slow timing information need be given to each module. Thus, the elapsed time counter on each module would record every pulse that it receives. A block diagram of such a design is shown in Figure 7.1.

This digital technique would have an advantage in that the computer software, and thus the computer operator, would be able to examine the elapsed time of each module in the system. This information could lead a serviceman to first run diagnostics on modules that were past their warranty period and perhaps significantly shorten the time required to isolate to a single faulty module. However, this digital technique has a limitation because once a module has been removed from a chassis, a serviceman has no way of telling the elapsed time of the module. The module must be plugged into some sort of tester that has a readout capability if a serviceman wished to determine if a module has passed its warranty period.

The digital technique would no doubt provide greater accuracy than the analog one. The accuracy of the analog approach is limited by the length of the tube and the precision with which the mercury's length can be plated and measured. An accuracy of one percent (100 hours in 10,000 hours) would be a typical example of the best commercial ones in use today. The digital timer's precision could easily show 10,000 or 15,000 hours down to the hour The accuracy is limited by the drift of the central chassis clock, but this would probably be a crystal with a typical accuracy of .01%. There also would be a small quantization error associated with the digital approach. The digital timers would take up more board space than the analog timer and use one module connector pin. The analog technique would use no connector pins. The digital timer requiring several integrated circuits would cost more.

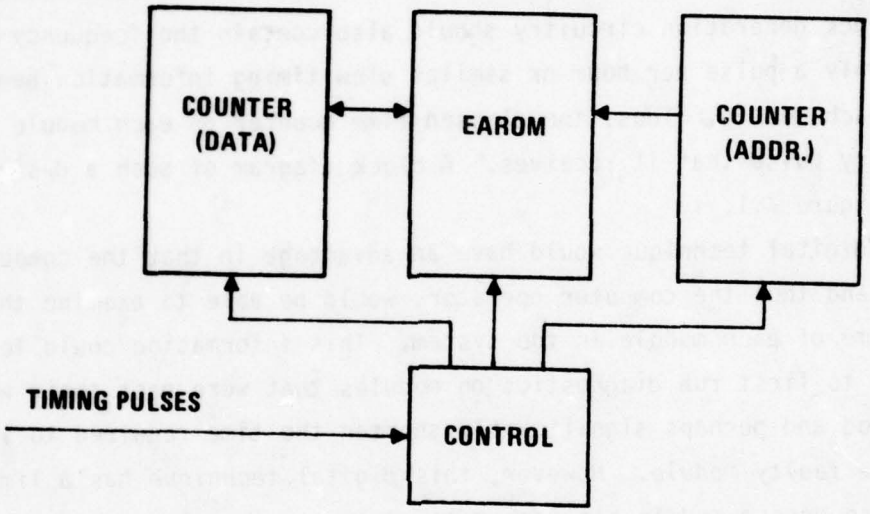


Figure 7.1 Elasped Time Indicator Block Diagram

In summary, the analog timer is small, inexpensive, and able to be read by visual inspection. The digital approach is very accurate and able to be read by the computer. A comparison of these two alternatives is shown in Table 7.1. A more detailed analysis of the required components and their possible environmental limitations needs to be done before a final specification is made. Perhaps by using both techniques, the advantages of each can be effectively used.

TABLE 7.1 COMPARISON OF ELAPSED TIME INDICATOR IMPLEMENTATIONS

Analog	Digital
- low cost	- moderate cost
- visually readable	- no visual readability
- no computer interface	- computer interface
- possible environmental problems	- rugged
- small size	- moderate size
- moderate accuracy	- very accurate

8.0 PERFORMANCE/COST EVALUATION OF THE RECOMMENDED BIT

This section deals with the quantitative assessment of the effectiveness of the built-in-tests recommended in the previous sections for the MCF AN/UYK-41(V) computer systems. Performance and cost of the recommended BIT have been evaluated in terms of the BIT effectiveness criteria discussed in Section 2.3.5.

It should be recalled that five BIT performance parameters and six BIT cost parameters were identified in Section 2.3.5. The performance parameters identified were: probability of detection (P_{SFD}), probability of localization (P_{LFE}), probability of false alarm (P_{FA}), time to detect (T_{SFD}), and time to localize (T_{LFE}). The BIT costs were categorized into hardware and software costs. The cost parameters identified were: space (A), power (P), and failure rate (FR) for the hardware, and operating system (OS), application software (AS), and diagnostic software (DS) for the software.

In order to meaningfully quantify these parameters it is necessary to identify a baseline system configuration whose characteristics are explicitly known. Then the impact of the BIT at the module, chassis, and system level can be ascertained relative to this baseline system configuration.

It should be emphasized that the MCF computer systems have not yet been designed and therefore functional logic diagrams are not yet available. The evaluation of the BIT performance and cost is based on the best available information at this time. The F^3 specifications permit a reasonably good engineering estimate of the BIT performance and cost at the module and chassis level. However, due to lack of information on the MCF software, the system level BIT performance and costs are difficult to estimate.

In the following sections, a baseline system is defined and then BIT approaches at the module, chassis, and system level are evaluated with respect to it. In the process of evaluating the BIT effectiveness a number of assumptions were made in order to quantify the performance and cost parameters listed above. These assumptions are explained in the sections where they are applicable.

8.1 Baseline System Definition

For purposes of the BIT effectiveness evaluation, the AN/UYK-41(V) single processor system has been chosen as the baseline system. It is assumed that this system consists of a Main Computer Chassis No. 1, one Memory Expansion Chassis, and one I/O Expansion Chassis. Furthermore, it is assumed that each chassis is populated with its full complement of modules. This forms a system with 256K words of memory and 14 MCF I/O channels which is assumed to be a typical single processor configuration [8].

A summary of the essential MCF module specifications are given in Table 8.1. They have been obtained from the F^3 specifications where available. Other parameters were estimated as explained in the notes. Of particular importance are the power dissipation and failure rate specifications which will be used for the purposes of the cost estimation of the baseline system.

The space requirements of digital circuits can be more easily compared in terms of the number of integrated circuit (IC) packages (or chips) than the physical dimensions of the modules. For this reason, the number of IC chips per MCF module was estimated using the physical dimensions of the modules as a basis. The Table 8.2 shows these estimates. The primary assumptions here are that each module consists of one or more printed circuit board(s). A more subtle assumption is that a major portion of the logic design is done with LSI circuits to increase the function density of each module. Other assumptions in deriving the chip count for modules are given in the notes on Table 8.2.

Using the information in Table 8.1 and 8.2, the space, power, and failure rate characteristics of the single processor are derived as shown in Table 8.3 and 8.4. Table 8.3 shows the cumulative totals for each chassis, while Table 8.4 shows the cumulative totals by the module type. The numbers given in these two tables are used in succeeding sections to determine the relative space, power, and failure rate increase due to additional BIT circuitry at the module, chassis, and system levels.

TABLE 8.1. SUMMARY OF RELEVANT MCF MODULE SPECIFICATIONS

Module Name	Module Type, Weight	Maximum Power Dissipation	MTBF hours	Failure Rate per 10^6 hours [1]
NRAM (32Kx18)	III 3.5 lbs.	70 W 25 W (Standby)	15,000	66.7
VRAM (32Kx18)	III 3.5 lbs.	50 W 40 W (Standby)	10,000	100
CPU3	IV 9.0 lbs.	80 W	6,000	166.7
MCM3	II 2.5 lbs.	30 W	40,000	25
BEM	II 3.0 lbs.	25 W	40,000	25
BIM2	II 3.0 lbs.	30 W	30,000	33.3
PCM2	V 12.0 lbs.	variable [2]	7,500	133.3
IOMOD	I 2.0 lbs.	20 W [3]	50,000 [4]	20

Notes

[1] Failure Rate $\lambda = \frac{10^6}{MTBF}$

[2] Power Dissipation of PCM2 based on 70% efficiency

[3] Estimated from I/O Expansion Chassis F^3 specifications

[4] Estimated from module type and maximum power dissipation.

TABLE 8.2. ESTIMATION OF TOTAL NUMBER OF IC CHIPS PER MCF MODULE

Module Name	Module Type	Dimensions Depth, Width, Height Inches	Estimated Number of Boards per Module [1]	Estimated Usable Area sq. inches [2]	Estimated Number of Chips [3]
VRAM32	III	1.4x9.0x6.0	3	140.25	140
CPU3	IV	3.5x9.0x7.17	7	327.25	245
MCM3	II	.95x9.0x6.48	2	93.5	70
BEM	II	.95x9.0x6.48	2	93.5	70
BIM2	II	.95x9.0x6.48	2	93.5	70
IOMOD	I	.45x9.0x6.48	1	46.75	35
PCM2	V	4.9x9.0x7.17	1	46.75	35 [4]

Notes:

[1] Assume .5 inch spacing between boards in module.

[2] Assume 8.5x.5 inches usable area per board.

[3] Assume .75 IC Chips/sq. inch density for Logic modules.
1.0 IC Chips/sq. inch density for Memory modules.

[4] Although PCM2 module may not have digital ICs, an equivalent number of ICs has been determined for the purpose of estimating space cost for the PCM BIT.

TABLE 8.3. SINGLE PROCESSOR SYSTEM CHARACTERISTICS
WITHOUT BUILT-IN-TEST BY CHASSIS
(DERIVED FROM F3 SPECIFICATIONS)

Chassis	Modules	Qty	Maximum Power Dissipation	Failure Rate / 10^6 hrs.	Number of Chips
Main Computer Chassis No. 1	VRAM32	2	100 W	200	280
	CPU3	1	80 W	166.7	245
	BEM	2	50 W	50	140
	BIM2	1	30 W	33.3	70
	IOMOD	4	80 W	80	140
	PCM2	1	145 W [1]	133.3	35 [2]
Subtotal		11	458 W	663.3	910
Percent			36.9%	36.3%	38.2%
Memory Expansion Chassis	BEM	1	25 W	25	70
	VRAM32	6	300 W	600	840
	PCM2	1	139 W [1]	133.3	35 [2]
Subtotal		8	464 W	758.3	945
Percent			35.4%	41.8%	39.7%
I/O Expansion Chassis	BEM	1	25 W	25	70
	BIM2	1	30 W	33.3	70
	IOMOD	10	200 W	200	350
	PCM2	1	109 W [1]	133.3	35 [2]
Subtotal		13	364 W	391.6	525
Percent			27.7%	21.6%	22.1%
Total		32	1313 W	1813.2	2380
Percent		100%	100%	100%	100%

Notes:

[1] Power dissipation of PCM2 based on 70% efficiency

[2] Equivalent number of chips.

TABLE 8.4. SINGLE PROCESSOR SYSTEM CHARACTERISTICS WITHOUT BUILT-IN-TEST BY MODULE (DERIVED FROM F^3 SPECIFICATIONS)

Module	VRAM32	CPU3	BEM	BIM2	IOMOD	PCM2	Total
Qty.	8	1	4	2	14	3	32
Maximum Power Dissipation	400 W	80 W	100 W	60 W	280 W	393 W [1]	1313 W
	30.5%	6.1%	7.6%	4.6%	21.3%	29.9%	100%
Failure Rate /10^6 hrs.	800	166.7	100	66.6	280	399.9	1813.2
	44.1%	9.2%	5.5%	3.7%	15.4%	22.1%	100%
Number of Chips	1120	245	280	140	490	105 [2]	2380
	47.0%	10.3%	11.8%	5.9%	20.6%	4.4%	100%

Notes:

[1] Power dissipation for PCM2 based on 70% efficiency.

[2] Equivalent number of chips.

8.2 Evaluation of Module Level BIT

The Module Level BIT as described earlier consists of fixed hardware for on-line fault detection and programmable hardware for idle time or off-line fault detection. The BIT hardware would be resident on the modules and would test the functional circuit on that module. At the module level there is no associated BIT software. Whatever software is required to use the programmable BIT hardware for fault detection is assumed to be at the chassis or the system level.

The cost of the BIT hardware at module level is estimated as follows. For each module, the recommended built-in-tests described in Section 6.0 were analyzed in detail. Recall that the built-in-tests were recommended based on the type of subfunctions within each module. Thus, for each BIT the number and type of IC chips required to test the subfunction partially or completely were determined. The power dissipation per chip was obtained from IC manufacturers and the failure rate data was obtained using MIL-HDBK-217. The total number of chips, maximum power dissipation and the total failure rate were then computed for each built-in-test. This detailed analysis is given in Appendix C. The hardware cost estimates are summarized in Table 8.5.

There are several problems associated with the cost estimates given in Table 8.5. 1) Because of the lack of detailed logic diagrams, the cost of not all of the recommended built-in-tests could be estimated. Where the cost could not be estimated, it was assumed to be zero which tends to lower the overall BIT cost figures. 2) On the other hand, for the built-in-tests for which the estimates could be made based on the functional specifications, the BIT hardware was estimated in terms of SSI and MSI chips. This is because the type of logic functions required for hardware testing are not currently available as LSI chips. This tends to increase the overall cost figures because it was assumed earlier that the functional circuits on the MCF modules are designed with LSI chips. These two factors partially compensate the errors in estimation of cost.

The Table 8.6 summarizes the performance/cost figures for the Module Level BIT. The hardware cost figures are taken directly from Table 8.5. The software costs are not applicable at the module level. In estimating

TABLE 8.5. HARDWARE COST ESTIMATION FOR MODULE LEVEL BIT ON MCF MODULES

Module	Type of BIT	Number of IC Chips		Maximum Power Dissipation		Failure Rate /10^6 hrs.	
VRAM32							
1) Data	a) Parity, or b) ECC	8 32		4.0 W 14.5 W		10.8 34.0	
2) R/W Control	a) Duplication	--		--		--	
Total		8	32	4.0	14.5	10.8	34.0
Percent Increase [1]		5.7%	22.9%	8%	29%	10.8%	-46.1% [2]
CPU3							
1) Clock	a) Maintenance clock b) Stepper clock	-- --		-- --		-- --	
2) µSequencer	a) Parity-µRegisters b) Support-µstep/break c) Illegal opcode	4 -- 2		1.6 W -- 0.1 W		0.97 -- 0.13	
3) Control Store	a) Parity b) µdiagnostic extension	11 5		3.3 W 2.5 W		2.78 2.81	
4) Timing & Control	a) Duplication	--		--		--	
5) Int. Data Paths	a) Parity-Int. Registers	15		5.9 W		3.98	
6) ALU	a) Residue code	--		--		--	
7) Control/Status Registers	a) Duplication	--		--		--	
8) CP Interface	a) MED	--		--		--	
9) MCF Bus Controller	a) Parity-data/address b) Timeouts	5 3		1.4 W 1.5 W		1.11 1.12	
10) ROM (256x36)	a) Parity	6		2.5 W		1.26	
Total		51		18.8 W		14.16	
Percent Increase [1]		20.8%		23.5%		21.2%	

-- Indicates BIT technique not used in cost/performance estimation.

TABLE 8.5. CONTINUED

Module	Type of BIT	Number of IC Chips	Maximum Power Dissipation	Failure Rate /10^6 hrs.
BEM	a) Parity-data/address b) Loop around	5 11	2.0 W 5.2 W	1.11 3.52
Total		16	7.2 W	4.63
Percent Increase [1]		22.9%	28.8%	18.5%
BIM2	a) Parity-data/address b) Parity-Int. registers c) Timeout d) Loop around	5 -- 2 6	2.0 W -- 1.0 W 2.7 W	1.11 -- 0.75 1.84
Total		13	5.7 W	3.70
Percent Increase [1]		18.6%	19%	11.1%
IOMOD	a) Parity-data/address b) Timeout c) Loop around	5 2 --	2.0 W 1.0 W --	1.11 0.75 --
Total		7	3.0 W	1.86
Percent Increase [1]		20%	15%	9.3%
PCM2	a) A/D + μP	5	1.5 W	1.35
Percent Increase [1]		14.3%	1.1% [3]	10.1%

Notes:

[1] Percent increases in space (A), power (P) and failure rate (FR) are calculated as follows:

$$A = \frac{\#\text{ of chips for BIT circuit/module}}{\text{Total \# of chips/module}}$$

$$P = \frac{\text{Max. power dissipation for BIT circuit/module}}{\text{Max. power dissipation/module}}$$

$$FR = \frac{\text{Failure rate for BIT circuit/module}}{\text{Total failure rate/module}}$$

[2] Failure rate for the memory module decreases due to the use of error correcting code. See details in Appendix C.

[3] Average of the maximum power dissipation for the PCM is 131 watts.

TABLE 8.6. SUMMARY OF PERFORMANCE/COST FIGURES FOR MODULE LEVEL BIT

Parameters	VRAM32	CPU3	BEM	BIM2	IOMOD	PCM2	Composite [1]
P_{SFD}	70%	40%	80%	60%	60%	95%	65.4%
T_{SFD}	1-2 μsec [2]						1-2 μsec
P_{FA}	0% [3]						0%
P_{LFE}	100% [4]						100%
T_{LFE}	1-2 μsec [5]						1-2 μsec
A	22.9%	20.8%	22.9%	18.6%	20%	14.3%	21.5%
P	29%	23.5%	28.8%	19%	15%	1.1%	16.9%
FR	-46.1% [6]	21.2%	18.5%	11.1%	9.3%	10.1%	-13.3%
OS	Not Applicable						N.A.
AS							N.A.
DS							N.A.

Notes:

[1] Composite figures are calculated for a single processor computer system given in Table 8.4 as follows:

Composite P_{SFD} = Σ (P_{SFD} of the module x percent distribution of failure rate for that type of module)

Composite A = Σ (A of the module x percent distribution of number of chips for that type of module)

Composite P = Σ (P of the module x percent distribution of the power dissipation for that type of module)

Composite FR = Σ (FR of the module x percent distribution of failure rate for that type of module)

TABLE 8.6. CONTINUED

Notes:

[2] Most module faults will be detected within one CPU instruction cycle time.

[3] It is assumed that false alarms can occur due to faulty BIT circuit. If the BIT circuit is faulty, it means the module is faulty. Therefore, the possibility of false alarms at module level is zero.

[4] Module Level BIT detects faults only within a module, i.e., detected faults are always localized to the module. Therefore, P_{LFE} = 100%.

[5] For the Module Level BIT fault detection and faults localization are synonymous functions.

[6] Failure rate of memory module reduces due to the use of error correcting code.

the performance figures several assumptions were made. These assumptions are noted in Table 8.6. The probability of fault detection (P_{SFD}) for the modules needs some clarification. The P_{SFD} is estimated based on the percentage of hardware functions monitored or tested by the BIT. Estimates were made for each module depending on the complexity of its subfunctions and the type of BIT circuits recommended for each subfunction.

The composite numbers given in the right-most column of Table 8.6 indicates the overall effectiveness of the Module Level BIT in the single processor system configuration.

8.3 Evaluation of the Chassis Level BIT

The Chassis Level BIT as described in the previous sections consist of microprocessor based intelligence which resides in a separate module within the chassis. It interfaces with a simple maintenance panel on the chassis and is responsible for testing all modules within the chassis.

For the purpose of estimating hardware costs it is assumed that such a tester can be implemented using hardware which is equivalent in complexity to a DEC LSI-11 microcomputer with 4K words of memory to store the diagnostic software. Table 8.7 lists the hardware cost for Chassis Level BIT using the LSI-11 microcomputer. The details of the components used and failure rate analysis are given in Appendix C. The power dissipation was obtained from the DEC Logic Handbook [27].

The cost impact of the Chassis Level BIT on each chassis differs slightly depending on the module complement within the chassis. The lower half of Table 8.7 shows the percent increases in space, power, and failure rate due to the Chassis Level BIT for each type of chassis.

For the Chassis Level BIT, diagnostic software must be developed. The type of diagnostic test routines required for each chassis will depend on the module complement within the chassis. It is assumed that very simple diagnostic routines will be used at the chassis level to perform functional tests on each module. An estimate was made of the type of tests required for each module and the number of instructions per test. From this the execution time required per test was estimated. The details of these estimates are given in Appendix C. The results are summarized in Table 8.8.

TABLE 8.7. HARDWARE COST ESTIMATION FOR CHASSIS LEVEL BIT

BIT Hardware	Number of Chips/ Components	Maximum Power Dissipation	Failure Rate /10^6 hrs.	Number Of Modules
Single board micro computer (LSI 11 or equivalent) with 4 KW random access memory	70	25.2 W	29.9	1
Chassis Maintenance Panel with switches and indicators	9	1.6 W	2.67	--
Total	79	26.8 W	32.6	1
Percent Increase: [1]	A	P	FR	A*
Main Computer Chassis No. 1	8.7%	5.5%	4.9%	9.1%
Memory Expansion Chassis	8.4%	5.8%	4.3%	12.5%
I/O Expansion Chassis	15%	7.4%	8.3%	7.7%

Notes:

[1] Percent Increase for space (A), power (P) and failure rate (FR) are calculated as follows:

$$A = \frac{\text{\# of chips for Chassis Level BIT/chassis}}{\text{Total \# of chips/chassis}}$$

$$A^* = \frac{\text{\# of modules for Chassis Level BIT/chassis}}{\text{Max. \# of modules/chassis}}$$

$$P = \frac{\text{Max. power dissipation for Chassis Level BIT/chassis}}{\text{Max. power dissipation/chassis}}$$

$$FR = \frac{\text{Failure rate for Chassis Level BIT/chassis}}{\text{Total failure rate/chassis}}$$

TABLE 8.8. DIAGNOSTIC SOFTWARE REQUIREMENTS FOR CHASSIS LEVEL BIT MODULE

Chassis	Diagnostic Test	Number of Instructions [1]	Max. Execution Time [2]	P_{SFD} [3]
Main Computer Chassis No. 1	Memory Test	1.5x150	2x1.4 sec	85%
	Basic CPU Test	1x250	1x2.5 msec	50%
	BEM Test	1.5x100	2x1.0 msec	90%
	BIM2 Test	1x100	1x1.0 msec	70%
	IOMOD Test	2.5x100	4x1.0 msec	70%
	PCM2 Test	--	--	95%
Total		975	2.8 sec	76% [4]
Memory Expansion Chassis	BEM Test	1x100	1x1.0 msec	90%
	Memory Test	3.5x150	6x1.4 sec	85%
	PCM2 Test	--	--	95%
Total		625	8.4 sec	86.9% [4]
I/O Expansion Chassis	BEM Test	1x100	1x1.0 msec	90%
	BIM2 Test	1x100	1x1.0 msec	70%
	IOMOD Test	5.5x100	10x1.0 msec	70%
	PCM2 Test	--	--	95%
Total		750	12.0 sec	79.8% [4]

Notes:

[1] Total Number of Instructions= $\frac{(N+1)}{2}$ x Number Instructions per Test
Where N= Number of Modules.

[2] Maximum Execution Time= N x Execution Time per Test
Where N= Number of Modules.

[3] Estimation includes the fault detection capability at module level.

[4] Total P_{SFD} calculated for a single processor computer system given in Table 8.3.
Total P_{SFD}= Σ (P_{SFD} for the module x percent distribution of failure rate for that type of module).

For detailed analysis on diagnostic software requirements refer to Appendix C.

In Table 8.8 the number of instructions and execution time per test have been multiplied by a factor which takes into account the number of modules using the same test software. The probability of fault detection (P_{SFD}) includes the fault detection capability of the Module Level BIT. This is because the Chassis Level BIT will exercise the modules using certain standard test patterns while the Module Level BIT will also be simultaneously checking the module hardware.

Finally, the performance/cost figures for the Chassis Level BIT are summarized in Table 8.9. The hardware and software cost figures are taken directly from Tables 8.7 and 8.8. The assumptions made in estimating the BIT performance are stated in the notes in Table 8.9. The composite numbers indicate the overall effectiveness of the Chassis Level BIT for the single processor system configuration.

8.4 Evaluation of the System Level BIT

The System Level BIT consists mainly of software routines to test the hardware in the whole system. This includes all modules, chassis, peripherals and their interconnecting buses. Such software is generally very extensive and runs under a diagnostic operating system in an off-line mode. There are several categories of software diagnostic programs such as system exercisers, subsystem (module in MCF context) exercisers, reliability tests, etc. Such tests typically require large amounts of memory and normally reside on external mass storage devices. It is difficult to evaluate the impact of additional hardware BIT on such off-line diagnostic software for several reasons. First, the hardware BIT is mainly geared towards on-line fault monitoring. Second, the specific diagnostic software code depends on the implementation of the hardware logic rather than the hardware F^3 specifications. Third, at this time only the architecture and not the detailed specifications for the MCF software are available. Although the AN/UYK-41(V) emulates the PDP-11/70 such that the time independent software written for the PDP-11/70 would be transferable to the AN/UYK-41 (V), it does not mean that the DEC PDP-11/70 diagnostic software can be meaningfully run on the AN/UYK-41(V).

In view of the above considerations, the evaluation of the System Level BIT has been restricted to software for the microdiagnostics and that

TABLE 8.9. SUMMARY OF PERFORMANCE/COST FIGURES FOR CHASSIS LEVEL BIT

Parameters	Main Computer Chassis No. 1	Memory Expansion Chassis	I/O Expansion Chassis	Composite [1]
P_{SFD}	76%	86.9%	79.8%	81.4%
T_{SFD} [2]	1.4 sec	4.2 sec	6.0 msec	4.2 sec
P_{FA} [3]	4.9%	4.3%	8.3%	5.4%
P_{LFE} [4]	100%	100%	100%	100%
T_{LFE} [2]	1.4 sec	4.2 sec	6.0 msec	4.2 sec
A	9%	8.7%	16.1%	10.5%
P	5.5%	5.8%	7.4%	6.1%
FR	4.9%	4.3%	8.3%	5.4%
OS	Not Applicable			N.A.
AS				N.A.
DS	975 Instructions	625 Instructions	750 Instructions	783 Instructions

Notes:

[1] Composite figures are calculated for a single processor computer system given in Table 8.3.

Composite P_{SFD} Σ (P_{SFD} of the chassis x percent distribution of failure rate for that type of chassis)

Composite T_{SFD}= T_{LFE}= Maximum of the three times.

Composite P_{FA} = Σ (P_{FA} of the chassis x percent distribution of failure rate for that type of chassis)

TABLE 8.9. CONTINUED

Composite A= Σ (A of the chassis x percent distribution of number of chips for that type of chassis)

Composite P= Σ (P of the chassis x percent distribution of power dissipation for that type of chassis)

Composite FR= Σ (FR of the chassis x percent distribution of failure rate for that type of chassis)

Composite DS= Average of the number of instructions

[2] It is assumed that on the average the time to detect and the time to localize the faults are the same because chassis level testing is predominantly off-time.

$T_{LFE} = T_{SFD}$ = 1/2 x Max. Total Execution Time

[3] It is assumed that the false alarms occur due to the failure of the Chassis Level BIT. Furthermore, it is assumed that every Chassis Level BIT failure result in a false alarm. Therefore, P_{FA} = FR.

[4] It is assumed that the Chassis Level BIT will test only one module at a time. Therefore, P_{LFE} = 100%.

portion of the macrodiagnostics that can be used for on-line or idle time testing.

Table 8.10 shows estimates of the microdiagnostic software requirements. Several test routines were considered which check mainly the hard core CPU logic and the accessibility of a portion of the memory where macrodiagnostics reside. The estimate for the execution time of the microdiagnostics includes several passes through the tests. The hardware requirements for the additional micromemory have already been included in the hardware cost estimates of the Module Level BIT for the CPU3 module.

The macrodiagnostics that are necessary to test a particular computer system are largely influenced by the actual hardware implementation. This is true of a computer system whether or not it is designed with BIT. It is beyond the scope of this report to quantify the software necessary to perform diagnostics on the MCF functional modules. Therefore, meaningful evaluation of the impact that built-in-test would have on the system level diagnostic software has not been included in this report. Table 8.11 shows the cost and performance estimates for the system level BIT that is contained in the microdiagnostic control store.

8.5 Summary of the Performance/Cost Evaluation

The performance/cost evaluation was done for the recommended built-in-tests at the module, chassis, and system levels. The performance and cost parameters were evaluated with respect to an MCF AN/UYK-41(V) single processor system configuration with 256K words of memory and 14 MCF I/O channels. The results of the BIT effectiveness evaluation are summarized in Table 8.12.

From this table it can be seen that the previously described BIT provides a high level of performance at a moderate cost. The probability that a fault will be detected by one of the three levels of BIT is estimated to be around 90%. Not only will faults be detected within about 4 seconds, but every fault that is detected will be localized to the faulty module within the same period of time. The probability of the BIT system indicating a module is faulty when it is not faulty is estimated to be less than 5%. The cost of this capability has been estimated in terms of space,

TABLE 8.10. MICRODIAGNOSTIC SOFTWARE REQUIREMENTS FOR THE SYSTEM LEVEL BIT

Diagnostic Test	Number of Microinstruction	Number of Passes	Maximum Execution Time [1]
Microsequencer Test	100	8	160 µsec
Register Test	150	8	240 µsec
ALU Test	400	8	640 µsec
Control Panel Test	200	8	320 µsec
MCF Bus Controller Test	300	32	1920 µsec
Memory Test	250	32	1600 µsec
Total	1150		4.88 µsec

Notes:

[1] Maximum execution time= Number of instruction x Number of passes x Average microinstruction execution time

Average microinstruction execution time assumed to be 200 nanoseconds

TABLE 8.11. SUMMARY OF PERFORMANCE/COST ESTIMATES FOR THE SYSTEM LEVEL BIT

Parameters	Micro-Diagnostics
P_{SFD}	90%
T_{SFD}	2.44 msec [1]
P_{FA}	0.15% [2]
P_{LFE}	100%
T_{LFE}	2.44 msec [1]
A	[3]
P	[3]
FR	[3]
OS	100 instructions
AS	Not Applicable
DS	1150 instructions

Notes:

[1] It is assumed that

$$T_{LFE} = T_{SFD} = 1/2 \times \text{Max. Total Execution Time for the Microdiagnostics.}$$

[2] It is assumed false alarms occur due to failure of the microdiagnostic control store. Furthermore, it is assumed that every diagnostic control store failure results in a false alarm. Therefore, P_{FA} = FR of the microdiagnostic control store.

[3] Cost of microdiagnostic hardware is included in the Module Level BIT for the CPU3 module.

TABLE 8.12. SUMMARY OF PERFORMANCE/COST ESTIMATES FOR THE MODULE, CHASSIS AND SYSTEM LEVEL BITS FOR A SINGLE PROCESSOR COMPUTER SYSTEM

Parameters	Module Level BIT	Chassis Level BIT	System Level BIT
P_{SFD}	65.4%	81.4% [1]	90% [1]
T_{SFD}	1-2 μsec	4.2 sec	2.44 msec
P_{FA}	0%	5.4%	0.15%
P_{LFE}	100%	100%	100%
T_{LFE}	1-2 μsec	4.2 sec	2.44 msec
A	21.5%	10.5%	[2]
P	16.9%	6.1%	[2]
FR	-13.3% [3]	5.4%	[2]
OS [4]	N.A.	N.A.	100
AS	N.A.	N.A.	N.A.
DS [4]	N.A.	783	1150

Notes:

[1] P_{SFD} at chassis and system level include the fault detection capability of the Module Level BIT.

[2] Cost of microdiagnostic hardware is included in the Module Level BIT for the CPU3 module.

[3] Negative failure rate increase is due to the use of error correcting code in the memory subsystem.

[4] Number indicate number of additional assembly language level instructions.

power, and failure rate increase. The space and power needed is about 25% more than the example system without BIT. However, due to the increased reliability of error-correcting code on the memory modules, the reliability of the total system with BIT is about 8% better than the same system without BIT. The impact on application programs is minimal and the added cost of diagnostic and operating system software is predicted to be quite small.

9.0 SUMMARY AND RECOMMENDED FURTHER WORK

The preceding sections of this report have discussed built-in-test as a means of accomplishing the Military Computer Family maintenance goals of 1) continuous system monitoring and indication of malfunction, 2) diagnosis of system malfunction to a module level with a low probability of a false module pull, and 3) measurement and recording of module elapsed time when a module is pulled. The approach taken in this study was to assume a fault population, predict where in the system these faults are most likely to occur and develop a rationale for deploying built-in fault detection and localization resources accordingly.

In the case of the AN/UYK-41(V) (PDP-11/70) configuration, at room temperature approximately 60% of all faults will occur in the memory, 30% will accrue in the CPU and 10% will exist in the remainder of the system. To detect and localize these faults with maximum probability of detection (P_{SFD}) and minimum additional maintenance hardware and software, a rationale was developed to show module, chassis and system level BIT should be used and that fault reporting would be from the lowest to the highest level of complexity. It was concluded using this approach that up to 80% of all faults can be detected with 10% additional hardware, 80-90% with 20% more hardware and 90-95% of all faults can be detected with 30% more hardware. To detect the remaining 5-10% and to minimize the probability of returning to vendor's modules which are not faulty, an on-site module/chassis off-line tester is recommended.

Since the ultimate outcome of this study will be amended MCF AN/UYK-41(V) form, fit and function specifications with built-in-test, the role of BIT at each level was characterized in terms of flexibility, intelligence, observability and operator accessibility. Various fault reporting schemes were evaluated with the requirement for minimizing false module pulls due to faulty checkers in mind. A summary of BIT functions at each level is given in Table 4.2.

During the course of this preliminary study of MCF built-in-test requirements and alternatives, a number of issues were identified which were beyond the scope of the present effort but which, nevertheless deserve some comment in the present work. The remainder of this section will be devoted to a discussion of these issues.

9.1 Fault Tolerant Aspects of MCF

Central to the MCF maintenance philosophy discussed in this report is the idea of on-line fault detection and isolation, and off-line manual repair through module replacement. This study has not specifically addressed the incorporation of fault tolerant computing techniques which lead to automatic fault detection, isolation, and on-line reconfiguration. While the emphasis of this study was not on fault tolerant computing as opposed to fault detection, isolation and repair, techniques, it does not mean that fault tolerance should be overlooked. It is recommended that in future studies emphasis be given to fault tolerant computing approaches. In particular, fault tolerant multi-processor hardware structures should be investigated.

9.2 On-Line BIT Relationship to Off-Line Automatic Test Equipment (ATE)

The present study has primarily addressed the question of what can be done with on-line fault monitoring facilities assuming a two-level maintenance philosophy. The study did not specifically consider tradeoffs between BIT and ATE from a system life cycle cost (LCC) standpoint. However, the study did recommend the use of some kind of off-line (but on-site) test facilities for minimizing the probability of returning non-faulty modules to vendors.

9.3 Implications of Future Very Large Scale Integrated (VLSI) Circuitry

Very large scale integrated circuitry will make possible the realization of even more complex functions within the bounds of the MCF form and fit specifications. One result of this could be the ability to include massive hardware redundancy on each module. Another consequence could be

multiprocessor hardware structures at very low cost which can effectively emulate prior generation machine while at the same time offer the fault tolerant benefits of inherently redundant structures.

9.4 Register Transfer Level BIT Simulations

Future work on BIT for MCF should include register-transfer (R-T) level simulations of MCF members with and without proposed BIT appraoches. Such simulations would be useful for verifying fault detection effectiveness and for predicting the amount of additional circuitry required for BIT.

REFERENCES

1. Coleman, A. H. and W. R. Smith, "The Military Computer Family: A New Joint-Service Approach to Military Computer Acquisition," Computer, Vol. 10, No. 10, October, 1977.

2. Barbacci, M. R. and D. P. Siewiorek, "Evaluation of CFA Test Programs via Formal Computer Descriptions," Computer, Vol. 10, No. 10, October, 1977.

3. Burr, W. E. and R. Gordon, "Selecting a Military Computer Architecture," Computer, Vol. 10, No. 10, October, 1977.

4. Fuller, S. M. and W. E. Burr, "Measurement and Evaluation of Alternative Architectures," Computer, Vol. 10, No. 10, October, 1977.

5. Avizienis, A., et. al., "The STAR (Self-Testing And Repairing) Computer: An Investigation of the Theory and Practice of Fault-Tolerant Computer Design," IEEE Transaction on Computers, Vol. C-20, No. 11, November, 1971.

6. Ritchie, A. E., Spencer, A. E., Tuomenoksa, L. S., No. 4 ESS: "System Objectives and Organization," Bell System Technical Journal, Vol. 56, No. 7, September, 1977, pp.1017-1028.

7. "PDP-11/60 Processor Handbook," Digital Equipment Corporation, 1977.

8. "AN/GYQ-21(V) Computer System Equipment Specifications for the Military Computer Family (MCF)," EL-SS-2838-MCF, prepared for U. S. Army CORADCOM by ITEK Corporation, 31 January 1978.

9. "AN/GYQ-21(V) Main Computer Chassis No. 1 Equipment Specification for the Military Computer Family (MCF)," EL-CP-2804-MCF, prepared for U. S. Army CORADCOM by ITEK Corporation, 31 January 1978.

10. "AN/GYQ-21(V) Main Computer Chassis No. 2 Equipment Specifications for the Military Computer Family (MCF)," EL-CP-2839-MCF, prepared for U. S. Army CORADCOM by ITEK Corporation, 31 January 1978.

11. "Memory Expansion Chassis Equipment Specification for the Military Computer Family (MCF)," EL-CP-2806-MCF, prepared for U. S. Army CORADCOM by ITEK Corporation, 31 January 1978.

12. "Input/Output Expansion Chassis Equipment Specification for the Military Computer Family (MCF), EL-CP-2807-MCF, prepared for U. S. Army CORADCOM by ITEK Corporation, 31 January 1978.

REFERENCES (Continued)

13. "General Chassis Equipment Specification for the Military Computer Family (MCF)," EL-SS-2800-MCF, prepared for U. S. Army CORADCOM by ITEK Corporation, 15 November 1977.

14. "General Module Equipment Specification for the Military Computer Family (MCF)," EL-SS-2801-MCF, prepared for U. S. Army CORADCOM by ITEK Corporation, 31 January 1978.

15. Tasar, O. and V. Tasar, "A Study of Intermittent Faults in Digital Computers," Proceeding of National Computer Conference, 1977.

16. Maestri, G. H., "The Retryable Processor," Proceedings of Fall Joint Computer Conference, 1972.

17. Ball, M. and F. Hardie, "Effect of Detection of Intermittent Failure in Digital Systems," Proceeding of Fall Joint Conference, 1969.

18. "The Uptime Leader," Digital Equipment Corporation, 1978.

19. "PDP-11/70 Processor Handbook," Digital Equipment Corporation, 1975.

20. "The PDP-11/70 Reliability and Maintainability (RAMP) Story," Digital Equipment Corporation.

21. "AN/AYK-14(V) Navy Standard Airborne Computer Technical Description," Control Data Corporation.

22. "Technical Report," Department of Computer Science, Carnegie-Mellon University, Pittsburg, PA.

23. "AN/GYQ-21(V) Central Processor Unit 3 Equipment Specification for the Military Computer Family (MCF)," EL-CP-2817-MCF, prepared for U. S. Army CORADCOM by ITEK Corporation, 31 January 1978.

24. "Computer Bus Architecture Specification for the Military Computer Family (MCF), EL-CG-2808-MCF, prepared for U. S. Army CORADCOM by ITEK Corporation, 31 January 1978.

25. "Bus Extender Module (BEM) Equipment Specification for the Military Computer Family (MCF), EL-CP-2824-MCF, prepared for U. S. Army CORADCOM by ITEK Corporation, 31 January 1978.

26. "Bus Interface Module 2 (BIM2) Equipment Specification for the Military Computer Family (MCF), EL-CP-2828-MCF, prepared for U. S. Army CORADCOM by ITEK Corporation, 31 January 1978.

27. "Logic Handbook," Digital Equipment Corporation, 1977.

APPENDIX A

DEFINITION OF TERMS*

*Most of these definitions were extracted from, "A Framework for Designing Testability into Electronic Systems," by W. L. Keiner, Naval Surface Weapons Center, Dahlgren, Virginia, May, 1978. The remaining definitions were generated as a part of the present study.

active test. One which generates its own test vectors, closed loop test.

automatic test equipment (ATE). Equipment that is designed to conduct analysis of functional or static parameters to evaluate the degree of performance degradation and that may be designed to perform fault isolation of unit malfunctions. The decision making, control, or evaluative functions are conducted with a minimum reliance upon human intervention. (MS1309B)

availability. A measure of the degree to which an item is in the operable and commitable state at the start of the mission, when the mission is called for at an unknown (random) point in time. (MS721B) Availability is the probability of system readiness over a long interval of time.

built-in-test (BIT). A test approach using BITE or self-test hardware or software to test all or part of the unit under test (UUT). (MS1309B)

built-in-test equipment (BITE). Any device which is part of an equipment or system and is used for the express purpose of testing that equipment or system. BITE is an identifiable unit of the equipment or system. (MS1309B)

casualty. A manifestation of a failure at the system level or major subsystem level such that the system/subsystem is incapable of performing its principal function(s). A casualty is differentiated from a malfunction by the greater seriousness or persistence of its nature.

catastrophic fault, analog. A fault in analog circuitry which causes a sudden change in operating characteristics which results in a complete lack of useful performance. (ATG)

catastrophic fault, digital. A primary failure in digital circuitry which causes secondary failures.

closed-loop testing. Testing in which the input stimulus is controlled by the equipment output monitor. (MS1309B)

confidence test. A go/no-go test.

controllability. An attribute of equipment design which defines or describes the extent to which signals of interest may be observed.

critical failure. A failure which results in a casualty.

diagnostic test. A test designed to perform fault isolation.

disruptive test. One which destroys (changes) the state of the hardware or software.

dynamic test. A test of one or more of the signal properties or characteristics of an equipment or any of its constituent items performed such that the parameters being observed are measured and assessed with respect to a specified time aperture or response. (ATG)

error. Any discrepancy between a computed, observed, or measured quantity and the true, specified, or theoretically correct value or condition. (IEEE)

external ATE. ATE which is physically separated from the unit under test when the UUT is in its operational environment.

failure. The termination of the ability of an item to perform its required function. (IEEE) A failure is the functional manifestation of a fault.

failure analysis. The logical, systematic examination of an item or its diagram(s) to identify and analyze the probability, causes, and consequences of potential and real failures. (MS721B)

failure mode. A failure classification.

failure universe/failure population. The failures which correspond to a selected fault population. This is used as a basis for the design and evaluation of tests.

false alarm. An indicated fault where no fault exists. (MS1309B)

false alarm rate. The frequency of occurrence of false alarms.

fault. A physical condition that causes a device, component, or element to fail to perform in a required manner; for example, a short-circuit or a broken wire. (IEEE)

fault coverage/failure coverage. An attribute of a test or test procedure expressed as the percent of faults of the failure population which that test or test procedure will detect.

fault detection. A process which discovers or is designed to discover the existence of faults; the act of discovering existence of a fault.

fault dictionary. A list of elements where each element consists of a test and all the faults detected by that test. (IEEE/FTC) Often only the LRUs which contain the faults are listed.

fault isolation. Where a fault is known to exist, a process which identifies or is designed to identify the location of that fault within a small number of relaceable units.

fault localization. Where a fault is known to exist, a process which identifies or is designed to identify the location of that fault within a general area of equipment. Fault localization may be less specific than fault isolation.

fault population. The totality of faults which may be incurred by a device.

fault prediction. A process used to predict that some component will be out of tolerance before the next scheduled maintenance period based upon the present measurement of component parameters.

fault signature. An output test vector resulting from the testing of a unit containing one or more faults.

fault tolerance. The capacity of a computer, subsystem, or program to withstand the effects of internal faults; the number of error-producing faults a computer, subsystem, or program can endure before normal functional capability is impaired. (IEEE/FTC)

functional fault. A fault which can be described by a change in function of some identifiable portion of a system. (IEEE/FTC) A failure.

functional modularity. The splitting of a system into parts or modules based on the function or purpose of these parts. (IEEE/FTC)

functional partitioning. The physical or electrical separation of system elements along interfaces which define and isolate these elements on bases of function or purpose.

functional test. A test which is intended to exercise an identifiable function of a system. (IEEE/FTC) The function is tested independent of the hardware implementing the function.

go/no-go test. A test designed to yield a "test pass" or "go" indication in the absence of faults in a UUT, and a "test fail" or "no-go" indication in the presence of fault(s).

hard core. That kernel of circuitry in a processor system which must be functioning properly in order for that processor or system to successfully execute tests of other portions of itself.

hard core failure. A failure in the hard core logic of a system which inhibits normal self-test of the system.

idle test time. Which occurs when the system (or resource) is idling.

initialize. (1) To establish an initial condition or starting state; for example, to set logic elements in a digital circuit or the contents of a storage location to a known state so that subsequent application of digital test patterns will drive the logic elements to another known state; and (2) to set counters, switches, and addresses to zero or other starting values at the beginning of, or at prescribed points in, a computer routine. (MS1309B)

input test vector. A test pattern.

interfering test. One which degrades the performance of the On-Line system (or resource) operation.

intermittent fault. A temporary fault. (IEEE)

inverted-pyramid/building-block. Descriptive terms characterizing a test or test technique whereby the smallest possible portions of hardware are tested first in the test sequence, and subsequent tests utilize previously verified hardware for execution.

latent fault time. The extent or duration of time during which an existing fault is undetected; the elapsed time between fault occurrence and fault detection.

line replaceable unit (LRU). A unit which is designated by the plan for maintenance to be removed upon failure from a larger entity (equipment, system) in the latter's operational environment. (MS1309B)

maintainability. A characteristic of equipment design and installation which is expressed as the probability that an item will be retained in or restored to a specified condition within a given period of time, when the maintenance is performed in accordance with prescribed procedures and resources. (MS721B)

malfunction. An error.

marginal fault. A failure such that some equipment function is impaired or out of tolerance and is of a nature such that catastrophic failure does not occur.

mean-time-between-maintenance (MTBM). The mean of the distribution of the time intervals between maintenance actions (either preventive, corrective, or both). (MS721B) Includes actions due to false alarms.

mean-time-to-isolate. The average time required to achieve fault isolation as measured from the time of fault detection to the time of fault isolation.

mean-time-to-localize. The average time required to achieve fault localization as measured from the time of fault detection to the time of fault localization.

mean-time-to-repair (MTTR). The total corrective maintenance time divided by the total number of corrective maintenance actions during a given period of time. (MS721B)

multiple failure. A joint occurrence of two or more single failures. (IEEE)

non-disruptive test. One which does not destroy (change) the state of the hardware or software.

non-interfering test. One which does not degrade the performance of the on-line system (or resource) operation.

observability. An attribute of equipment design which defines or describes the extent to which signals of interest may be observed.

off-line test. One which occurs when the system (or resource) is off-line.

on-line test. One which occurs concurrent with the on-line operation of the system (or resource) on-line tests are either continuous or sampled (which occur periodically).

passive test. One which does not generate its own test vectors, open loop test.

periodic test. Off-line test which occurs periodically.

random fault/random failure. An intermittent fault whose occurrence is predictable only in a statistical sense.

readiness. A state of being ready to successfully perform or being in the act of successfully performing a defined mission.

readiness test. A test specifically designed to determine whether an equipment or system is operationally suitable for a mission. (MS1309B)

reconfiguration. A repair strategy in which failing components are switched out of operation and replaced by failure-free components. (IEEE/FTC)

recovery. The continuation of system operation with error-free data after an error occurs. (IEEE/FTC)

redundance, redundancy. The introduction of auxiliary elements and components into a system to perform the same functions as other elements in the system for the purpose of improving reliability and safety. (IEEE) Also, the use of additional components, programs, or repeated operations, not normally required by the system to execute its specified tasks, to overcome the effects of failures. (IEEE/FTC)

repeatability. A test characteristic such that repeated application of a given set of stimuli to a UUT yields identical results.

resource (module) on-line. When it is being used by the system.

resource (module) off-line. When it is not being used by the system and is not scheduled to be used.

resource (module) idling. When it is not being used by the system but is scheduled to be used.

solid fault. A permanent fault. (IEEE)

stuck fault/stuck failure. A failure in which a digital signal is permanently held in one of its binary states. (IEEE)

symptom. The manifestation or evidence of a particular failure condition.

system on-line. When some of the resources (modules) are being used for the applications.

system off-line. When none of the resources (modules) are being used for the application and none are scheduled to be used.

system idling. When none of the resources (modules) are being used for the application but some are scheduled to be used.

test. A procedure or action taken to determine under real or simulated conditions the capabilities, limitations, characteristics, effectiveness, reliability, or suitability of a material, device, system, or method. (MS1309B)

test pattern. A simultaneous or parallel definition of all the inputs of a system. (IEEE/FTC)

test point. A node within a circuit or system which can be measured or stimulated to facilitate testing.

transient failure. A failure induced by a momentary or temporary external factor such as input power fluctuation, excessive ambient temperature excursion, electromagnetic interference, or by factors internal to a system. A solid fault may cause a transient failure.

APPENDIX B

FAILURE RATE ANALYSES

COMPUTED USING AUTOFAIL PROGRAM

PDP11/70.REL LSI= 16.000 ROM= 16.000 RAM= 16.000

[illegible] = 1.000 B = 16.000 L = 1.000 I = 25.000

MODULE	FAILURE RATE	PERCENTAGE
	603.119	100.000
PDP-11/70	11.389	1.888
DATA.PATH	9.757	1.618
ALU.CONTROL	13.516	2.241
IR.DECODE	2.558	.424
CONSOLE	18.499	3.067
PROCESSOR.DATA.AND.UNIBUS.REGS	17.773	2.947
MICROSEQUENCER	5.711	.947
TIMING.GENERATOR	9.915	1.644
TRAP.AND.MSC.CONTROL	12.138	2.013
UNIBUS.AND.CONSOLE.CONTROL	16.726	2.773
ADDRESS.MEMORY.BOARD	17.546	2.909
CACHE.CONTROL	17.370	2.880
CACHE.DATA.PATH	14.457	2.397
DATA.MEMORY	14.020	2.325
SYSTEM.ADDRESS.PATH	11.625	1.928
SYS.DESC/CNSL.CABLES	13.313	2.207
SYSTEM.STATUS.REGISTER	12.027	1.994
UNIBUS.MAP	26.005	4.312
FRACTION.PROCESSOR.LOW.ORDER	14.697	2.437
FP.ROM.CONTROL	22.810	3.783
FRACTION.PROCESSOR.EXPON.PATH	24.936	4.135
ALL.FRACTION.PROC.HIGH.ORDER	74.111	12.288
16K.MEMORY	74.111	12.288
16K.MEMORY	74.111	12.288
16K.MEMORY	74.111	12.288
16K.MEMORY		

# of chips = 2342.000 # of gates = 24170.000 # of bits = 1146912.000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	1202.000	146.133	.244
MSI	668.000	161.656	.268
LSI	.000	.000	.000
ROM	50.000	9.074	.015
RAM	414.000	285.956	.474
MOS	256.000	271.849	.451
BIP	2006.000	331.271	.549

xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

E = 1.000 Q = 16.000 L = 1.000 T = 40.000

MODULE	FAILURE RATE	PERCENTAGE
PDP-11/70	1048.298	100.000
DATA.PATH	12.761	1.217
ALU.CONTROL	11.256	1.074
IR.DECODE	14.195	1.354
CONSOLE	2.806	.268
PROCESSOR.DATA.AND.UNIBUS.REGS	21.309	2.033
MICROSEQUENCER	21.094	2.012
TIMING.GENERATOR	6.292	.600
TRAP.AND.MSC.CONTROL	10.964	1.046
UNIBUS.AND.CONSOLE.CONTROL	13.542	1.292
ADDRESS.MEMORY.BOARD	20.489	1.955
CACHE.CONTROL	19.755	1.884
CACHE.DATA.PATH	19.[illegible]85	1.878
DATA.MEMORY	19.074	1.820
SYSTEM.ADDRESS.PATH	16.[illegible]37	1.587
SYS.DESC/CNSL.CABLES	12.958	1.236
SYSTEM.STATUS.REGISTER	15.436	1.472
UNIBUS.MAP	14.776	1.410
FRACTION.PROCESSOR.LOW.ORDER	30.832	2.941
FP.ROM.CONTROL	17.384	1.658
FRACTION.PROCESSOR.EXPON.PATH	27.659	2.638
ALL.FRACTION.PROC.HIGH.ORDER	29.553	2.819
16K.MEMORY	172.460	16.451
16K.MEMORY	172.460	16.451
16K.MEMORY	172.460	16.451
16K.MEMORY	172.460	16.451

# of chips = 2342.000 # of gates = 24170.000 # of bits = 1146912.000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	1202.000	160.204	.153
MSI	668.000	191.375	.183
LSI	.000	.000	.000
ROM	58.000	13.358	.013
RAM	414.000	683.361	.652
MOS	256.000	662.325	.632
BIP	2086.000	385.973	.368

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

E = 1.000 Q = 16.000 L = 1.000 T = 60.000

MODULE	FAILURE RATE	PERCENTAGE
PDP-11/70	2832.022	100.000
DATA.PATH	16.429	.580
ALU.CONTROL	15.144	.535
IR.DECODE	18.579	.656
CONSOLE	3.468	.122
PROCESSOR.DATA.AND.UNIBUS.REGS	28.593	1.010
MICROSEQUENCER	29.595	1.045
TIMING.GENERATOR	7.847	.277
TRAP.AND.MSC.CONTROL	13.727	.485
UNIBUS.AND.CONSOLE.CONTROL	17.255	.609
ADDRESS.MEMORY.BOARD	30.084	1.062
CACHE.CONTROL	25.571	.903
CACHE.DATA.PATH	25.727	.908
DATA.MEMORY	30.755	1.086
SYSTEM.ADDRESS.PATH	23.339	.824
SYS.DESC/CNSL.CABLES	16.469	.582
SYSTEM.STATUS.REGISTER	20.908	.738
UNIBUS.MAP	19.815	.700
FRACTION.PROCESSOR.LOW.ORDER	43.125	1.523
FP.ROM.CONTROL	24.279	.857
FRACTION.PROCESSOR.EXPON.PATH	39.973	1.411
ALL.FRACTION.PROC.HIGH.ORDER	41.485	1.465
16K.MEMORY	584.963	20.655
16K.MEMORY	584.963	20.655
16K.MEMORY	584.963	20.655
16K.MEMORY	584.963	20.655

# of chips = 2342.000 # of gates = 24170.000 # of bits = 1146912.000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	1202.000	197.025	.070
MSI	668.000	267.937	.095
LSI	.000	.000	.000
ROM	58.000	24.089	.009
RAM	414.000	2342.971	.827
MOS	256.000	2304.577	.814
BIP	2086.000	527.445	.186

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

E = 1.000 Q = 16.000 L = 1.000 T = 85.000

MODULE	FAILURE RATE	PERCENTAGE
PDP-11/70	10755.451	100.000
DATA.PATH	26.466	.246
ALU.CONTROL	25.451	.237
IR.DECODE	30.286	.282
CONSOLE	5.280	.049
PROCESSOR.DATA.AND.UNIBUS.REGS	47.894	.445
MICROSEQUENCER	51.821	.482
TIMING.GENERATOR	12.099	.112
TRAP.AND.MSC.CONTROL	21.181	.197
UNIBUS.AND.CONSOLE.CONTROL	27.300	.254
ADDRESS.MEMORY.BOARD	55.063	.512
CACHE.CONTROL	41.235	.383
CACHE.DATA.PATH	41.856	.389
DATA.MEMORY	60.895	.566
SYSTEM.ADDRESS.PATH	40.871	.380
SYS.DESC/CNSL.CABLES	25.934	.241
SYSTEM.STATUS.REGISTER	35.322	.328
UNIBUS.MAP	33.130	.308
FRACTION.PROCESSOR.LOW.ORDER	75.671	.704
FP.ROM.CONTROL	42.353	.394
FRACTION.PROCESSOR.EXPON.PATH	71.948	.669
ALL.FRACTION.PROC.HIGH.ORDER	73.001	.679
16K.MEMORY	2477.599	23.036
16K.MEMORY	2477.599	23.036
16K.MEMORY	2477.599	23.036
16K.MEMORY	2477.599	23.036

# of chips = 2342.000 # of gates = 24170.000 # of bits = 1146912.000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	1202.000	297.763	.028
MSI	668.000	469.487	.044
LSI	.000	.000	.000
ROM	58.000	51.479	.005
RAM	414.000	9936.722	.924
MOS	256.000	9854.028	.916
DIP	2086.000	901.423	.084

xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

I8080.REL LSI= 16.000 ROM= 16.000 RAM= 16.000

E = 1.000 Q = 16.000 L = 1.000 T = 25.000

MODULE	FAILURE RATE	PERCENTAGE
INTEL.8080.BOARD	9.176	100.000

# of chips = 17.000 # of gates = 1740.000 # of bits = 40960.000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	.000	.000	.000
MSI	6.000	1.927	.210
LSI	1.000	.762	.083
ROM	2.000	2.866	.312
RAM	8.000	3.621	.395
MOS	11.000	7.250	.790
BIP	6.000	1.927	.210

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

E = 1.000 Q = 16.000 L = 1.000 T = 40.000

MODULE	FAILURE RATE	PERCENTAGE
INTEL.8080.BOARD	10.850	100.000

# of chips = 17.000 # of gates = 1740.000 # of bits = 40960.000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	.000	.000	.000
MSI	6.000	2.414	.122
LSI	1.000	1.628	.082
ROM	2.000	6.898	.347
RAM	8.000	8.911	.449
MOS	11.000	17.436	.878
BIP	6.000	2.414	.122

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

E = 1.000 Q = 16.000 L = 1.000 T = 60.000

MODULE	FAILURE RATE	PERCENTAGE
INTEL.8080.BOARD	63.913	100.000

# of chips = 17.000 # of gates = 1740.000 # of bits = 40960.000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	.000	.000	.000
MSI	6.000	3.634	.057
LSI	1.000	5.268	.082
ROM	2.000	23.854	.373
RAM	8.000	31.157	.487
MOS	11.000	60.279	.943
BIP	6.000	3.634	.057

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

E = 1.000 Q = 16.000 L = 1.000 T = 85.000

MODULE	FAILURE RATE	PERCENTAGE
INTEL.8080.BOARD	263.976	100.000

# of chips = 17.000 # of gates = 1740.000 # of bits = 40960.000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	.000	.000	.000
MSI	6.000	6.750	.026
LSI	1.000	22.004	.083
ROM	2.000	101.801	.386
RAM	8.000	133.421	.505
MOS	11.000	257.226	.974
BIP	6.000	6.750	.026

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

F8.REL LSI= .000 ROM= 16.000 RAM= 16.000

E = 1.000 Q = 16.000 L = 1.000 T = 25.000

MODULE	FAILURE RATE	PERCENTAGE
F.8.POWER.SUPPL MICROPROCESSOR	3.510	100.000
PROCESSOR	2.782	79.247
A/D	.493	14.041
OCTAL.LATCH	.236	6.712

# of chips = 3.000 # of gates = 6415.000 # of bits = .000

TYPE	# of CHIPS	FAILURE RATE	PERCENTAGE
SSI	.000	.000	.000
MSI	1.000	.236	.067
LSI	2.000	3.275	.933
ROM	.000	.000	.000
RAM	.000	.000	.000
MOS	2.000	3.275	.933
BIP	1.000	.236	.067

E = 1.000 Q = 16.000 L = 1.000 T = 40.000

MODULE	FAILURE RATE	PERCENTAGE
F.8.POWER.SUPPLY.MICROPROCESSOR	7.448	100.000
PROCESSOR	6.135	82.363
A/D	1.044	14.012
OCTAL.LATCH	.270	3.624

# of chips = 3.000 # of gates = 6415.000 # of bits = .000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	.000	.000	.000
MSI	1.000	.270	.036
LSI	2.000	7.178	.964
ROM	.000	.000	.000
RAM	.000	.000	.000
MOS	2.000	7.178	.964
BIP	1.000	.270	.036

E = 1.000 Q = 16.000 L = 1.000 T = 60.000

MODULE	FAILURE RATE	PERCENTAGE
F.8.POWER.SUPPLY.MICROPROCESSOR	23.958	100.000
PROCESSOR	20.236	84.465
A/D	3.360	14.025
OCTAL.LATCH	.362	1.510

# of chips = 3.000 # of gates = 6415.000 # of bits = .000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	.000	.000	.000
MSI	1.000	.362	.015
LSI	2.000	23.597	.985
ROM	.000	.000	.000
RAM	.000	.000	.000
MOS	2.000	23.597	.985
BIP	1.000	.362	.015

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

F = 1.000 Q = 16.000 L = 1.000 T = 85.000

MODULE	FAILURE RATE	PERCENTAGE
F.8.POWER.SUPPLY.MICROPROCESSOR	99.684	100.000
PROCESSOR	85.062	85.331
A/D	14.009	14.054
OCTAL.LATCH	.613	.615

# of chips = 3.000 # of gates = 6415.000 # of bits = .000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	.000	.000	.000
MSI	1.000	.613	.006
LSI	2.000	99.071	.994
ROM	.000	.000	.000
RAM	.000	.000	.000
MOS	2.000	99.071	.994
BIP	1.000	.613	.006

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

LSI11.REL LSI= 16.000 ROM= 16.000 RAM= 16.000

E = 1.000 Q = 16.000 L = 1.000 T = 25.000

MODULE	FAILURE RATE	PERCENTAGE
LSI11	29.893	100.000
SPECIAL.FUNTIONS	.669	2.237
BUS.ARBITRATION.LOGIC	.350	1.172
INTERRUPT.CONTROL.AND.RESET.LOGIC	.776	2.596
CLOCK.PULSE.GENERATOR	.851	2.847
ROM.CHIPS	3.413	11.416
DATA.CHIP	1.160	3.880
CONTROL.CHIP	1.160	3.880
BUS.DRIVERS.AND.RECIEVERS	1.588	5.314
MEMORY	16.991	56.837
BUS.I/O.CONTROL.LOGIC	1.500	5.019
I/O.BUS.MEM.READ.DATA.MUX	1.195	3.999
FAST.DIN.MUX	.241	.805

# of chips = 68.917 # of gates = 7145.083 # of bits = 99328.000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	37.250	4.899	.164
MSI	10.667	2.272	.076
LSI	2.000	2.320	.078
ROM	3.000	3.413	.114
RAM	16.000	16.991	.568
MOS	21.000	22.723	.760
BIP	47.917	7.171	.240

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

E = 1.000 Q = 16.000 L = 1.000 T = 40.000

MODULE	FAILURE RATE	PERCENTAGE
LSI11	62.660	100.000
SPECIAL.FUNTIONS	.745	1.190
BUS.ARBITRATION.LOGIC	.390	.622
INTERRUPT.CONTROL.AND.RESET.LOGIC	.868	1.386
CLOCK.PULSE.GENERATOR	.927	1.480
ROM.CHIPS	8.237	13.146
DATA.CHIP	2.510	4.005
CONTROL.CHIP	2.510	4.005
BUS.DRIVERS.AND.RECIEVERS	1.769	2.823
MEMORY	41.395	66.063
BUS.I/O.CONTROL.LOGIC	1.710	2.729
I/O.BUS.MEM.READ.DATA.MUX	1.330	2.123
FAST.DIN.MUX	.269	.430

# of chips = 68.917 # of gates = 7145.083 # of bits = 99328.000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	37.250	5.388	.086
MSI	10.6[illegible]	2.621	.042
LSI	2.000	5.019	.080
ROM	3.000	8.237	.131
RAM	16.000	41.395	.661
MOS	21.000	54.652	.872
[illegible]	47.917	8.009	.128

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

E = 1.000 Q = 16.000 L = 1.000 T = 60.000

MODULE	FAILURE RATE	PERCENTAGE
LSI11	199.168	100.000
SPECIAL.FUNTIONS	.951	.477
BUS.OPERATION.LOGIC	.495	.249
INTERRUPT.CONTROL.AND.RESET.LOGIC	1.114	.559
CLOCK.PULSE.GENERATOR	1.131	.568
ROM.CHIPS	28.527	14.323
DATA.CHIP	8.187	4.111
CONTROL.CHIP	8.187	4.111
BUS.DRIVERS.AND.RECIEVERS	2.251	1.130
MEMORY	144.036	72.319
BUS.I/O.CONTROL.LOGIC	2.254	1.131
I/O BUS.MEM.READ.DATA.MUX	1.691	.849
FAST.DIN.MUX	.345	.173

# of chips = 68.917 # of gates = 7145.083 # of bits = 99328.000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	37.250	6.696	.034
MSI	10.667	3.535	.018
LSI	2.000	16.374	.082
ROM	3.000	28.527	.143
RAM	16.000	144.036	.723
MOS	21.000	188.937	.949
BIP	47.917	10.231	.051

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

E = 1.000 Q = 16.000 L = 1.000 T = 85.000

MODULE	FAILURE RATE	PERCENTAGE
LSI11	822.509	100.000
SPECIAL.FUNTIONS	1.512	.184
BUS.ARBITRATION.LOGIC	.784	.095
INTERRUPT.CONTROL.AND.RESET.LOGIC	1.778	.216
CLOCK.PULSE.GENERATOR	1.688	.205
ROM.CHIPS	121.803	14.809
DATA.CHIP	34.285	4.168
CONTROL.CHIP	34.285	4.168
BUS.DRIVERS.AND.RECIEVERS	3.570	.434
MEMORY	615.877	74.878
BUS.I/O.CONTROL.LOGIC	3.697	.449
I/O.BUS.MEM.READ.DATA.MUX	2.677	.325
FAST.DIN.MUX	.554	.067

# of chips = 68.917 # of gates = 7145.083 # of bits = 99328.000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	37.250	10.276	.012
MSI	10.667	5.984	.007
LSI	2.000	68.569	.083
ROM	3.000	121.803	.148
RAM	16.000	615.877	.749
MOS	21.000	806.249	.980
LIF	47.917	16.260	.020

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

PP1170.RIL ISI= 16.000 ROM= 16.000 RAM= 16.000

I = 1.000 R = 16.000 L = 1.000 T = 25.000

MODULE	FAILURE RATE	PERCENTAGE
PDP-11/70.WITH.CONSOLE.RIT	633.013	100.000
PDP-11/70	603.119	95.278
DATA.PATH	11.389	1.808
ALU.CONTROL	9.757	1.618
IR.DECODE	12.516	2.075
CONSOLE	2.558	.424
PROCESSOR.DATA.AND.UNIBUS.REGS	18.499	3.067
MICROSEQUENCER	17.773	2.947
TIMING.GENERATOR	5.711	.947
TRAP.AND.MSC.CONTROL	9.915	1.644
UNIBUS.AND.CONSOLE.CONTROL	12.138	2.013
ADDRESS.MEMORY.BOARD	16.726	2.773
CACHE.CONTROL	17.546	2.909
CACHE.DATA.PATH	17.370	2.880
DATA.MEMORY	14.457	2.397
SYSTEM.ADDRESS.PATH	14.020	2.325
SYS.DESC/CNSL.CABLES	11.625	1.928
SYSTEM.STATUS.REGISTER	13.313	2.207
UNIBUS.MAP	12.827	2.127
FRACTION1.PROCESSOR.LOW.ORDER	26.085	4.325
FP.RUN.CONTROL	14.697	2.437
FRACTION.PROCESSOR.EXPON.PATH	22.010	3.703
ALL.FRACTION.PROC.HIGH.ORDER	24.936	4.135
TAG.MEMORY	74.111	12.288
TAG.MEMORY	74.111	12.288
TAG.MEMORY	74.111	12.288
TAG.MEMORY	74.111	12.288
LSI11	29.893	4.722
SPECIAL.FUNCTIONS	.669	2.237
BUS.ARBITRATION.LOGIC	.350	1.172
INTERRUPT.CONTROL.AND.RESET.LOGIC	.776	2.596
CLOCK.PULSE.GENERATOR	.851	2.847
ROM.CHIPS	3.413	11.416
DATA.CHIP	1.160	3.880
CONTROL.CHIP	1.160	3.880
BUS.DRIVERS.AND.RECEIVERS	1.588	5.314
MEMORY	16.991	56.837
BUS.I/O.CONTROL.LOGIC	1.500	5.019
I/O.BUS.DEM.READ.DATA.MUX	1.195	3.999
FAST.DIN.MUX	.241	.805

# of chips = 2410.917 # of gates = 31315.083 # of bits = 1246240.000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	1239.250	151.432	.239
MSI	670.667	163.928	.259
LSI	2.000	2.320	.004
ROM	61.000	12.187	.020
RAM	430.000	302.947	.479
MOS	272.000	294.522	.465
BIP	2133.917	338.441	.535

E = 1.000 B = 16.000 L = 1.000 T = 40.000

MODULE	FAILURE RATE	PERCENTAGE
PDP-11/70.WITH.CONSOLE.BIT	1110.958	100.000
PDP-11/70	1048.298	94.360
DATA.PATH	12.761	1.217
ALU.CONTROL	11.256	1.074
IR.DECODE	14.195	1.354
CONSOLE	2.806	.268
PROCESSOR.DATA.AND.UNIBUS.REGS	21.309	2.033
MICROSEQUENCER	21.094	2.012
TIMING.GENERATOR	6.292	.600
TRAP.AND.MSC.CONTROL	10.964	1.046
UNIBUS.AND.CONSOLE.CONTROL	13.542	1.292
ADDRESS.MEMORY.BOARD	20.489	1.955
CACHE.CONTROL	19.755	1.884
CACHE.DATA.PATH	19.685	1.878
DATA.MEMORY	19.074	1.820
SYSTEM.ADDRESS.PATH	16.637	1.587
SYS.DESC/CNSL.CABLES	12.958	1.236
SYSTEM.STATUS.REGISTER	15.436	1.472
UNIBUS.MAP	14.776	1.410
FRACTION.PROCESSOR.LOW.ORDER	30.832	2.941
FP.ROM.CONTROL	17.384	1.658
FRACTION.PROCESSOR.EXPON.PATH	27.659	2.638
ALL.FRACTION.PROC.HIGH.ORDER	29.553	2.819
16K.MEMORY	172.460	16.451
16K.MEMORY	172.460	16.451
16K.MEMORY	172.460	16.451
16K.MEMORY	172.460	16.451
LSI11	62.660	5.640
SPECIAL.FUNTIONS	.745	1.190
MOS.ARBITRATION.LOGIC	.390	.622
INTERRUPT.CONTROL.AND.RESET.LOGIC	.868	1.386
CLOCK.PULSE.GENERATOR	.927	1.480
ROM.CHIPS	8.237	13.146
DATA.CHIP	2.510	4.005
CONTROL.CHIP	2.510	4.005
MOS.DRIVERS.AND.RECIEVERS	1.769	2.823
MEMORY	41.395	66.063
MOS.I/O.CONTROL.LOGIC	1.710	2.729
I/O.MUS.MEM.READ.DATA.MUX	1.330	2.123
FAST.DIN.MUX	.269	.430

# of chips = 2410.917 # of gates = 31315.083 # of bits = 1246240.000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	1239.250	165.592	.149
MSI	670.667	193.996	.175
LSI	2.000	5.019	.005
ROM	41.000	21.595	.019
RAM	430.000	724.756	.652
MOS	777.000	716.926	.645
BIP	2133.217	193.980	.305

E = 1.000 U = 14.000 L = 1.000 T = 60.000

MODULE	FAILURE RATE	PERCENTAGE
PDP-11/70.WITH.CONSOLE.BIT	3031.190	100.000
PDP-11/70	2832.022	93.429
DATA.PATH	16.429	.580
ALU.CONTROL	15.144	.535
IR.DECODE	18.579	.656
CONSOLE	3.468	.122
PROCESSOR.DATA.AND.UNIBUS.REGS	28.593	1.010
MICROSEQUENCER	29.595	1.045
TIMING.GENERATOR	7.847	.277
TRAP.AND.MSC.CONTROL	13.727	.485
UNIBUS.AND.CONSOLE.CONTROL	17.255	.609
ADDRESS.MEMORY.BOARD	30.084	1.062
CACHE.CONTROL	25.571	.903
CACHE.DATA.PATH	25.727	.908
DATA.MEMORY	30.755	1.086
SYSTEM.ADDRESS.PATH	23.339	.824
SYS.MISC/CONSL.CABLES	16.469	.582
SYSTEM.STATUS.REGISTER	20.908	.738
UNIBUS.MAP	19.815	.700
FRACTION.PROCESSOR.LOW.ORDER	43.125	1.523
FP.ROM.CONTROL	24.279	.857
FRACTION.PROCESSOR.EXPON.PATH	39.973	1.411
ALL.FRACTION.PROC.HIGH.ORDER	41.485	1.465
16K.MEMORY	584.963	20.655
16K.MEMORY	584.963	20.655
16K.MEMORY	584.963	20.655
16K.MEMORY	584.963	20.655
LSI11	199.168	6.571
SPECIAL.FUNTIONS	.951	.477
BUS.ARBITRATION.LOGIC	.495	.249
INTERRUPT.CONTROL.AND.RESET.LOGIC	1.114	.559
CLOCK.PULSE.GENERATOR	1.131	.568
ROM.CHIPS	20.527	14.323
DATA.CHIP	8.187	4.111
CONTROL.CHIP	8.187	4.111
BUS.DRIVERS.AND.RECIEVERS	2.251	1.130
MEMORY	144.036	72.319
BUS.I/O.CONTROL.LOGIC	2.254	1.131
I/O.BUS.MEM.READ.DATA.MUX	1.691	.849
FAST.4TH.MUX	.345	.173

# of chips = 2410.917 # of gates = 31315.083 # of bits = 1246240.000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	1239.250	264.722	.067
MSI	670.667	271.472	.090
LSI	2.000	16.474	.005
ROM	61.000	52.617	.017
RAM	430.000	2487.097	.820
MPU	27.000	2493.515	.823
PIO	2133.917	537.676	.177

E = 1.000 U = 16.000 L = 1.000 T = 85.000

MODULE	FAILURE RATE	PERCENTAGE
PDP-11/70.WITH.CONSOLE.BIT	11577.959	100.000
PDP-11/70	10755.451	92.896
DATA.PATH	26.466	.246
ALU.CONTROL	25.451	.237
IR.DECODE	30.286	.282
CONSOLE	5.280	.049
PROCESSOR.DATA.AND.UNIBUS.REGS	47.894	.445
MICROSEQUENCER	51.821	.482
TIMING.GENERATOR	12.099	.112
TRAP.AND.MSC.CONTROL	21.181	.197
UNIBUS.AND.CONSOLE.CONTROL	27.300	.254
ADDRESS.MEMORY.BOARD	55.063	.512
CACHE.CONTROL	41.235	.383
CACHE.DATA.PATH	41.856	.389
DATA.MEMORY	60.895	.566
SYSTEM.ADDRESS.PATH	40.871	.380
SYS.RESL/CNSL.CABLES	25.934	.241
SYSTEM.STATUS.REGISTER	35.322	.328
UNIBUS.MAP	33.130	.308
FRACTION.PROCESSOR.LOW.ORDER	75.671	.704
FP.ROM.CONTROL	42.353	.394
FRACTION.PROCESSOR.EXPON.PATH	71.948	.669
ALL.FRACTION.PROC.HIGH.ORDER	73.001	.679
16K.MEMORY	2477.599	23.036
16K.MEMORY	2477.599	23.036
16K.MEMORY	2477.599	23.036
16K.MEMORY	2477.599	23.036
LSI11	822.509	7.104
SPECIAL.FUNTIONS	1.512	.104
BUS.ARBITRATION.LOGIC	.784	.095
INTERRUPT.CONTROL.AND.RESET.LOGIC	1.778	.216
CLOCK.PULSE.GENERATOR	1.680	.205
ROM.CHIPS	121.003	14.809
DATA.CHIP	34.285	4.168
CONTROL.CHIP	34.285	4.168
BUS.DRIVERS.AND.RECIEVERS	3.570	.434
MEMORY	615.877	74.878
BUS.I/O.CONTROL.LOGIC	3.697	.449
I/O.BUS.MEM.READ.DATA.MUX	2.677	.325
FAST.BIN.MUX	.554	.067

# of chips = 2410.917 # of gates = 31315.083 # of bits = 1246240.000

TYPE	# of CHIPS	FAILURE RATES	PERCENTAGE
SSI	1239.250	308.039	.027
MSI	678.667	475.471	.041
LSI	2.000	60.569	.006
RAM	61.000	173.281	.015
ROM	130.000	10552.599	.911
MOS	277.000	10660.277	.921
BIP	2133.917	917.683	.079

```
[PDP-11/70
   [DATA.PATH
     5F,7400
     42F,7404
     5F,7410
     11F,7411
     2F,7420
     1F,7464
     36,74153
     9,74153
     2,74157
     3,74182]
   [ALU.CONTROL
     11F,7400
     41F,7404
     26F,7405
     13F,7410
     20F,7411
     4F,7420
     11F,7464
     2F,7450
     2F,7474
     2F,7430
     2F,74112
     4,74153
     10,74158
     2,74174
     2,74169
     4,74189
     1,74288
     8,3101]
   [IR.DECODE
     24F,7474
     45F,7404
     2F,7440
     3F,7464
     2,74157
     5,8251
     23F,7410
     7F,DM8881
     43F,7400
     47F,7411
     8F,7464
     6F,7450
     10F,7420
     4,74153
     5F,7465
     1F,7405
     2,MK8192]
[CONSOLE
     19F,7400
     55F,7404
     3F,DM8881
     12F,7417
     1,DM9318]
[PROCESSOR.DATA.AND.UNIBUS.REGS
     24,74153
     47F,7404
     3F,7400
     12,74174
     4,7485
     2F,7440
     16F,7474
     16F,DM8881
     13F,7401
     2,74175
     1,DM9318
     7F,7410
     3F,7411
     2F,7420
     2F,7450
     1,74157
     16F,DM8640]
[MICROSEQUENCER
     12,74174
     17,3601
     67F,7404
     9F,7411
     28F,7474
     1,74175
     37F,7464
     33F,7410
     10F,7400
     6F,7420
     2F,7440
     4,74153]
[TIMING.GENERATOR
     6,7440
     8,74112
     5,7404
     7,7474
     5,7400
     2,7465
     4,7464
     2,7411
     2,74140
     2,7420]
```

```
[TRAP.AND.NSC.CONTROL
  6,7400
  12,7404
  7,7410
  19,7411
  8,7420
  4,7430
  2,7440
  4,7450
  4,7464
  4,7474
  4,74112
  1,74153
  3,74174
  1,DM8640
  2,DM8881]
[UNIBUS.AND.CONSOLE.CONTROL
  2,7430
  2,7450
  4,DM8881
  13,7400
  9,7404
  3,7410
  9,7411
  3,7420
  16,7474
  4,74112
  4,74140
  1,74157
  5,74123
  1,74193
  1,DM8881
  2,7442
  2,74175
  4,DM8640]
[ADDRESS.MEMORY.BOARD
  1,7474
  2,74193
  1,7400
  4,7404
  1,7410
  2,7411
  1,7464
  9,74140
  14,74153
  15,DM8881
  7,74175
  9,DM8262
  2,DM8640
  6,7485
  30,93410]
[CACHE.CONTROL
  2,7450
  4,74157
  8,74151
  4,74153
  1,7442
  1,7437
  1,74123
  13,7400
  7,7404
  6,7410
  10,7411
  2,7420
  11,7464
  13,7474
  18,74112
  2,74140
  2,74175
  1,74133
  5,74174
  1,DM8640]
[CACHE.DATA.PATH
  4,74157
  5,7400
  4,7404
  5,7410
  6,7411
  2,7420
  4,7464
  6,7474
  2,74140
  9,74158
  18,DM8881
  12,74175
  18,DM8881
  6,DM8262
  11,DM8640]
[DATA.MEMORY
  8,7404
  10,74153
  72,93410
  4,DM8262
  3,7400
  18,7440
  5,7464]
```

```
[SYSTEM.ADDRESS.PATH
  1,7421
  1,7437
  4,7408
  2,7485
  8,74181
  5,7400
  9,7404
  1,7405
  2,7410
  11,7411
  3,7420
  6,7440
  6,7464
  3,7474
  3,74153
  7,74157
  3,74158
  2,74182
  24,3101]
[SYS.DESC/CNSL.CABLES
  1,7474
  3,7404
  5,DM8881
  1,8815
  7,7401
  2,7483
  7,74153
  3,7408
  2,7400
  12,7404
  1,7410
  9,7411
  5,7420
  1,7440
  3,7464
  3,74158
  2,74174
  1,74155
  2,74157
  10,74133
  2,74157
  5,7474]
[SYSTEM.STATUS.REGISTER
  8,74153
  1,7442
  2,7437
  1,7408
  6,7400
  9,7404
  4,7410
  8,7411
  3,7405
  5,7440
  8,7464
  3,74157
  8,74174
  4,74175
  1,74157
  8,7474
  4,3601]
[UNIBUS.MAP
  7,74157
  3,74174
  12,DM8881
  3,74153
  2,7474
  5,74181
  9,7404
  1,74182
  1,7450
  4,7411
  3,7400
  2,7430
  2,7420
  5,DM8881
  10,DM8640
  2,7485
  1,7405
  3,7440
  1,74158
  1,7410]
```

```
[FRACTION.PROCESSOR.LOW.ORDER
  1,DM8242
  8,74153
  8,74181
  2,7400
  2,7404
  1,7410
  3,7411
  3,74153
  5,74157
  7,74158
  11,74174
  3,74175
  17,74157
  3,74182
  7,74189
  34,74148
  1,36011
[FP.ROM.CONTROL
  3,74151
  1,7486
  1,74193
  9,7400
  8,7404
  7,7410
  4,7411
  2,7420
  9,7440
  3,7464
  9,7474
  3,74112
  7,74140
  3,74174
  1,74157
  4,74151
  5,74175
  5,7451
  1,7442
  14,36011
```

```
[FRACTION.PROCESSOR.EXPON.PATH
  2,DM8242
  1,74151
  8,74153
  2,7485
  3,74181
  5,7400
  2,7404
  6,7405
  5,7410
  3,7411
  3,7420
  3,74140
  17,74153
  1,7474
  1,7464
  14,74174
  15,74175
  1,74157
  2,7451
  1,74133
  3,74158
  6,74189
  1,74182
  12,36011
[ALL.FRACTION.PROC.HIGH.ORDER
  1,DM8242
  7,74181
  3,7400
  4,7404
  2,7410
  3,7411
  1,7474
  5,74153
  17,74157
  7,74158
  12,74174
  3,74157
  3,74175
  1,7451
  1,7485
  7,74189
  2,74148
  2,74182
  30,74148
  2,36011
4[MEM16]
```

```
BLOCK.MEMORY
  2,7493
  1,7483
  5,7400
  1,7403
  2,7410
  1,7420
  1,74140
  3,74153
  3,7474
  2,DM8640
  5,DM8641
  1,74138
  1,74133
  3,74128
  2,7402
  5,7475
  2,7437
  64,MK40963
```

```
[LSI11
  [SPECIAL.FUNTIONS
    2F,DM8641
    3F,7474
    1 ,7442
    5F,7404
    1F,7400]
  [BUS.ARBITRATION.LOGIC
    1F,7400
    1F,DM8837
    3F,7474
    1F,DM8641]
  [INTERRUPT.CONTROL.AND.RESET.LOGIC
    4F,7404
    4F,7474
    2F,DM8641
    2F,7400
    5F,DM8837
    1F,7405
    1F,74174]
  [CLOCK.PULSE.GENERATOR
    1F,7400
    1F,74140
    2F,7474
    1F,74139
    6F,7404
    4F,MH0026]
  [ROM.CHIPS
    3 ,CP1631B]
  [DATA.CHIP
    1 ,CP1611B]
  [CONTROL.CHIP
    1 ,CP1621B]
  [BUS.DRIVERS.AND.RECIEVERS
    4 ,74257
    4 ,DM8641
    1F,DM8641
    4F,7411
    2F,7405]
  [MEMORY
    16,MK4096]

[BUS.I/O.CONTROL.LOGIC
  1F,7497
  7F,7400
  7F,7404
  2F,7411
  4F,7474
  5F,7410
  5F,DM8641
  1F,DM8837]
[I/O.BUS.MEM.READ.DATA.MUX
  4F,7475
  2F,74257
  3F,7410
  3F,7400
  2F,74140
  2F,7405
  2F,74107]
[FAST.DIN.MUX
  1F,74257
  1F,7400
  1F,7404]]
```

```
[F.8.POWER.SUPPLY.MICROPROCESSOR
[PROCESSOR
1,3870]
[A/D
1,8703]
[OCTAL.LATCH
1,9348]]
```

```
[INTEL.8080.BOARD
  1,8080
  6,8212
  8,8101
  2,8316]
```

APPENDIX C

BUILT-IN-TEST

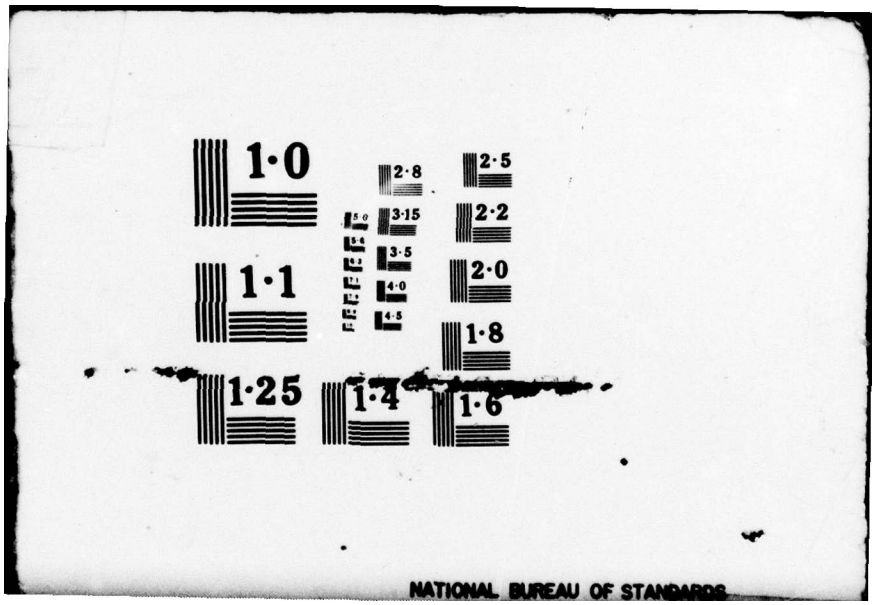
COST MEASUREMENT TABLES FOR MCF MODULES

This appendix contains the listings of the type and approximate number of packages necessary to implement the BIT techniques discussed in this report. Along with this information is the failure rate (FR) and the maximum power consumption for each of the integrated circuits. The failure rate data was obtained from the reliability analysis computer program at Carnegie-Mellon University. A temperature of 25°C was used so as to get data that was comparable with the module failure rate as specified in the ITEK documents. The maximum power consumption data was generally obtained from manufacturer's data sheets. After the information on the hardware cost estimates is the information on the software costs.

AD-A067 744 BATTELLE COLUMBUS LABS OHIO F/G 9/2
A PRELIMINARY STUDY OF BUILT-IN-TEST FOR THE MILITARY COMPUTER --ETC(U)
MAR 79 J B CLARY, A JAI, S WEIKEL, R SOEKS DAAG29-76-D-0100
UNCLASSIFIED CORADCOM-76-0100-F NL

3 OF 3
ADA
067744

END
DATE
FILMED
6-79
DDC


1·0
1·1
1·25
1·4
1·6
2·8
3·15
3·5
4·0
4·5
2·5
2·2
2·0
1·8
NATIONAL BUREAU OF STANDARDS

MODULE: VRAM32

BIT TECHNIQUE: SINGLE ERROR CORRECTION WITH DOUBLE ERROR DETECTION

Part Name	Part Number (Typical)	Quantity	Maximum Power Per IC (mw)	F.R. per IC (/10^6 hours)
16K x 1 RAM	MK16384	12	750	2.49
Parity Gen/Check	DM8262	7	300	.236
4-to-16 Line Decoder	54154	2	350	.251
Multiplexer	54257	3	250	.191
Exclusive-OR	5486	4	275	.191
Misc. Control	54XX	4	200	.165
MODULE TOTAL		32	14.5w	34.03*

*With no considerations for fault tolerance.
Effective Module Failure Rate with ECC as shown above is 53.9 /10^6 hours.

MODULE: VRAM32

BIT TECHNIQUE (ALTERNATE): BYTE PARITY

Part Name	Part Number (Typical)	Quantity	Maximum Power Per IC (mw)	F.R. per IC ($/10^6$ hours)
16K x 1 RAM	MK16384	4	750	2.49
Parity Gen/Check	DM8262	2	300	.236
Misc. Control	54XX	2	200	.165
MODULE TOTAL		8	4.0w	10.76

MODULE: CPU3

Part Name	Part Number (Typical)	Quantity	Maximum Power Per IC (mw)	F.R. per IC (/10^6 hours)
FUNCTION: REGISTERS				
BIT TECHNIQUE: PARITY				
Register File	54170	3	500	.478
Parity Gen/Check	DM8262	8	450	.236
Misc. Control	54XX	4	200	.165
FUNCTION TOTAL		15	5.9w	3.98
FUNCTION: CONTROL STORE				
BIT TECHNIQUE: PARITY				
2K x 4 ROM	TMS4700	1	500	.561
Parity Gen/Check	DM8262	8	300	.236
Misc. Control	54XX	2	200	.165
FUNCTION TOTAL		11	3.3w	2.78

MODULE: CPU3 (Continued)

Part Name	Part Number (Typical)	Quantity	Maximum Power Per IC (mw)	F.R. per IC ($/10^6$ hours)
FUNCTION: MICROSEQUENCER REGISTERS				
BIT TECHNIQUE: PARITY				
Latch	9308	1	500	.335
Parity Gen/Check	DM8262	2	450	.236
Misc. Control	54XX	1	200	.165
FUNCTION TOTAL		4	1.6w	.97
FUNCTION: BUS DATA AND ADDRESS				
BIT TECHNIQUE: PARITY				
Parity Gen/Check	DM8262	4	300	.236
Misc. Control	54XX	1	200	.165
FUNCTION TOTAL		5	1.4w	1.11

MODULE: CPU3 (Continued)

Part Name	Part Number (Typical)	Quantity	Maximum Power Per IC (mw)	F.R. per IC ($/10^6$ hours)
FUNCTION: MICRODIAGNOSTIC CONTROL STORE				
BIT TECHNIQUE: PARITY				
2Kx4 ROM	TMS4700	5	500	.561
FUNCTION TOTAL		5	2.5w	2.81
FUNCTION: TIMING				
BIT TECHNIQUE: WATCHDOG TIMER				
Counter (4-bit)	54192	1	500	.373
FUNCTION TOTAL (3 Timers)		3	1.5w	1.12
FUNCTION: ROM STORAGE				
BIT TECHNIQUE: PARITY				
256x4 ROM	54187	1	500	.153
Parity Gen/Check	DM8262	4	450	.263
Misc. Control	54XX	1	200	.155
FUNCTION TOTAL		6	2.5w	1.26

MODULE: CPU3 (Continued)

Part Name	Part Number (Typical)	Quantity	Maximum Power Per IC (mw)	F.R. per IC ($/10^6$ hours)
FUNCTION: OP-CODE				
BIT TECHNIQUE: ILLEGAL OP-CODE CHECK				
NAND (8-input)	5430	2	50	.066
FUNCTION TOTAL		2	.1w	.13
MODULE TOTAL		51	18.8w	14.16

MODULE: BEM

Part Name	Part Number (Typical)	Quantity	Maximum Power Per IC (mw)	F.R. per IC ($/10^6$ hours)
FUNCTION: BUFFER				
BIT TECHNIQUE: PARITY				
Parity Gen/Check	DM8262	4	450	.236
Misc. Control	54XX	1	200	.165
FUNCTION TOTAL		5	2.0w	1.11
FUNCTION: CONTROL				
BIT TECHNIQUE: LOOP AROUND				
Latches	9308	10	500	.335
Misc. Control	54XX	1	200	.165
FUNCTION TOTAL		11	5.2w	3.52
MODULE TOTAL		16	7.2w	4.63

MODULE: BIM2

Part Name	Part Number (Typical)	Quantity	Maximum Power Per IC (mw)	F.R. per IC ($/10^6$ hours)
FUNCTION: BUFFER				
BIT TECHNIQUE: PARITY				
Parity Gen/Check	DM8262	4	450	.236
Misc. Control	54XX	1	200	.165
FUNCTION TOTAL		5	2.0w	1.11
FUNCTION: CONTROL				
BIT TECHNIQUE: WATCHDOG TIMER				
Counter (4-bit)	54192	1	500	.373
FUNCTION TOTAL (2 Timers)		2	1.0w	.75
FUNCTION: UNIBUS CONTROL				
BIT TECHNIQUE: LOOP AROUND				
Latches	9308	5	500	.335
Misc. Control	54XX	1	200	.165
FUNCTION TOTAL		6	2.7w	1.84
MODULE TOTAL		13	5.7w	3.70

MODULE: I/O MODULE

Part Name	Part Number (Typical)	Quantity	Maximum Power Per IC (mw)	F.R. per IC ($/10^6$ hours)
FUNCTION: BUFFER				
BIT TECHNIQUE: PARITY				
Parity Gen/Check	DM8262	4	450	.236
Misc. Control	54XX	1	200	.165
FUNCTION TOTAL		5	2.0w	1.11
FUNCTION: CONTROL				
BIT TECHNIQUE: WATCHDOG TIMER				
Counter (4-bit)	54192	1	500	.373
FUNCTION TOTAL (2 Timers)		2	1.0w	.75
MODULE TOTAL		7	3.0w	1.86

MODULE: PCM2

Part Name	Part Number (Typical)	Quantity	Maximum Power Per IC (mw)	F.R. per IC ($/10^6$ hours)
BIT TECHNIQUE: MICROPROCESSOR PLUS A/D				
Microprocessor	3870	1	750	2.8
A/D	8703	1	250	.5
Latch	74S373	1	500	.2
Sensors	-	1*	-	7
Discretes	-	1*	-	3
MODULE TOTAL		5	1.5w	13.5

*Equivalent on the basis of board space.

CHASSIS MAINTENANCE PANEL

Part Name	Part Number (Typical)	Quantity	Maximum Power Per IC (mw)	F.R. per IC ($/10^6$ hours)
Switches DPDT	-	5	-	.15
Alpha-Numeric Display	-	4	400	.48
TOTAL		9	1.6w	2.67

CHASSIS LEVEL SOFTWARE COSTS

MODULE	NUMBER OF INSTRUCTION	EXECUTION TIME [1]
RAM		
- Memory Data Test	50	350,000 cycles
- Memory Controller Test	50	50 cycles
- Memory Address Test	50	350,000 cycles
TOTAL	150	1.4 sec
CPU		
- Register Test	50	1,000 cycles
- Basic Instruction Test	200	250 cycles
TOTAL	250	2.5 msec
BEM		
- Parity Check Test	50	250
- Loop Around Test	50	250
TOTAL	100	1.0 msec
BIM2		
- Parity Check Test	50	250
- Loop Around Test	50	250
TOTAL	100	1.0 msec
I/O MODULES		
- Parity Check Test	50	250
- Loop Around Test	50	250
TOTAL	100	1.0 msec

NOTE:

[1] Execution time computed by multiplying number of cycles by a typical microprocessor cycle time of 2 microseconds.